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2. Explain the working of a
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5. How does LED differ from an ordinary diode ?
6. What is a photo-diode ?
7. How does photo-diode work ?
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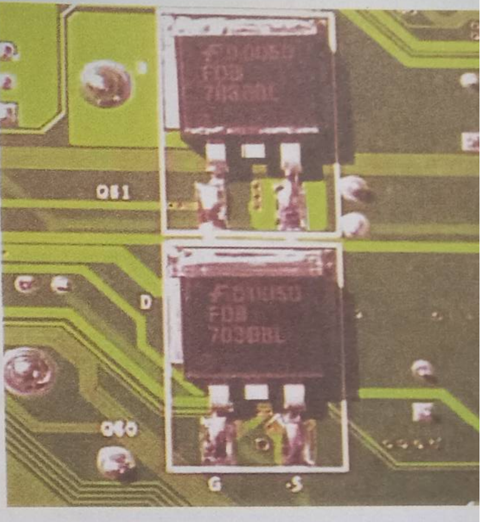
9. What is an optoisolator ?
10. What is a tunnel diode ?
11. Explain the V-I characteristics of a tunnel diode.
12. Explain the working of tunnel diode oscillator.
13. What is a varactor diode ?
14. Explain the working of varactor diode.
15. Give one application of varactor diode.
16. Explain the working of Shockley diode.

Discussion Questions

1. Why is LED not made of silicon or germanium ?
2. Where do we use seven-segment display ?
3. How do we protect LED from large reverse voltage ?
4. How does photo-diode differ from an ordinary diode ?
5. What is dark resistance of photo-diode ?
6. What do you mean by the sensitivity of photo-diode ?
7. What is the use of optoisolator ?
8. How does the width of depletion layer change the capacitance of a varactor ?

Transistors



INTRODUCTION

When a third doped element is added to a crystal diode in such a way that two *pn* jur are formed, the resulting device is known as a *transistor*. The transistor—an entire type of electronic device—is capable of achieving amplification of weak signa fashion comparable and often superior to that realised by vacuum tubes. Transistors are far than vacuum tubes, have no filament and hence need no heating power and may be operated position. They are mechanically strong, have practically unlimited life and can do some job than vacuum tubes.

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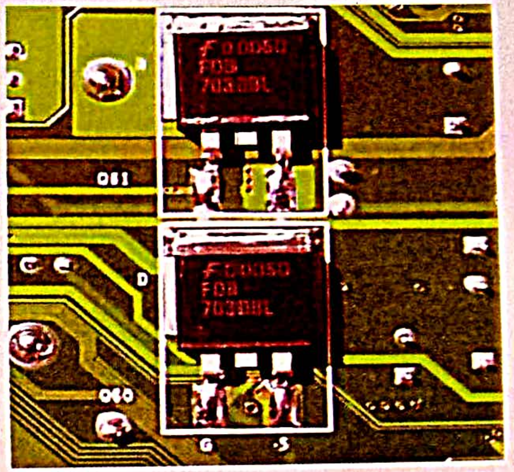
Transistors



TRODUCTION

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Invented in 1948 by J. Barde... most electronic ap... ...ough transistor sistor has now become the heart of most electronic... replacing vacuum tubes in almost all applications more than 58 years old, yet it is fast replacing vacuum tubes in almost all applications we shall focus our attention on the various aspects of transistors and their increasing the fast developing electronics industry.

8.1 Transistor

A **transistor** *consists of two pn junctions formed by *sandwiching either p-type or n-type semicon*ductor between a pair of opposite types. Accordingly ; there are two types of transistors

(*i*) *n-p-n* transistor (*ii*) *p-n-p* transistor

An *n-p-n* transistor is composed of two *n*-type semiconductors separated by a thin section of *p*-type as shown in Fig. 8.1 (*i*). However, a *p-n-p* transistor is formed by two *p*-sections separated by a thin section of *n*-type as shown in Fig. 8.1 (*ii*).

Fig. 8.1

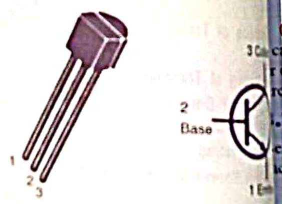
In each type of transistor, the following points may be noted :

(*i*) These are two *pn* junctions. Therefore, a transistor may be regarded as a combin... diodes connected back to back.

(*ii*) There are three terminals, one taken from each type of semiconductor.

(*iii*) The middle section is a very thin layer. This is the most important factor in the fu... transistor.

Origin of the name "Transistor". When new devices are invented, scientists often try to devise a name that will appropriately describe the device. A transistor has two *pn* junctions. As discussed later, one junction is forward biased and the other is reverse biased. The forward biased junction has a low resistance path whereas a reverse biased junction has a high resistance path. The weak signal is introduced in the low resistance circuit and output is taken from the high resistance circuit. Therefore, a transistor *transfers* a signal from a low resistance to high resistance. The prefix 'trans' means the signal transfer property of the device while 'istor' classifies it as a solid element in the same gene... with resistors.



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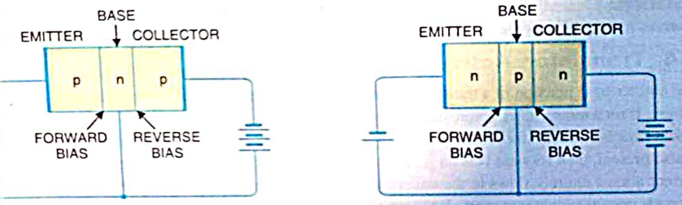
* In practice, these three blocks *p*, *n*, *p* are grown out of the same crystal by adding corresponding ... in turn.

Naming the Transistor Terminals

...nsistor (*pnp* or *npn*) has three sections of doped semiconductors. The section on one side is the ...er and the section on the opposite side is the *collector*. The middle section is called the *base* and ...s two junctions between the emitter and collector.

(*i*) **Emitter.** The section on one side that supplies charge carriers (electrons or holes) is ...ed the *emitter*. *The emitter is always forward biased w.r.t. base* so that it can supply a ... number of *majority carriers. In Fig. 8.2 (*i*), the emitter (*p*-type) of *pnp* transistor is forward ...ed and supplies hole charges to its junction with the base. Similarly, in Fig. 8.2 (*ii*), the ...ter (*n*-type) of *npn* transistor has a forward bias and supplies free electrons to its junction with the ...

(*ii*) **Collector.** The section on the other side that collects the charges is called the *collector*. *The ...ector is always reverse biased.* Its function is to remove charges from its junction with the base. ...ig. 8.2 (*i*), the collector (*p*-type) of *pnp* transistor has a reverse bias and receives hole charges that ...w in the output circuit. Similarly, in Fig. 8.2 (*ii*), the collector (*n*-type) of *npn* transistor has reverse ...s and receives electrons.



(*i*) (*ii*)

Fig. 8.2

(*iii*) **Base.** The middle section which forms two *pn*-junctions between the emitter and collector ...called the *base*. The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector ...rcuit.

.3 Some Facts about the Transistor

...efore discussing transistor action, it is important that the reader may keep in mind the following ...cts about the transistor :

(*i*) The transistor has three regions, namely ; *emitter*, *base* and *collector*. The base is much ...inner than the emitter while **collector is wider than both as shown in Fig. 8.3. However, for the ...ake of convenience, it is customary to show emitter and collector to be of equal size.

(*ii*) The emitter is heavily doped so that it can inject a large number of charge carriers (electrons ...or holes) into the base. The base is lightly doped and very thin ; it passes most of the emitter injected ...charge carriers to the collector. The collector is moderately doped.

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* Holes if emitter is *p*-type and electrons if the emitter is *n*-type.

** During transistor operation, much heat is produced at the collector junction. The collector is made larger to dissipate the heat.

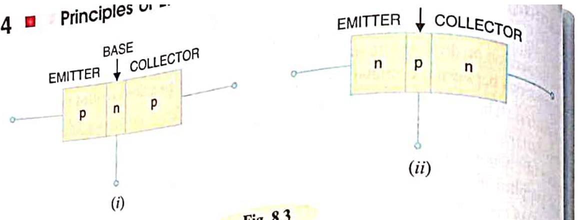


Fig. 8.3

(*iii*) The transistor has two *pn* junctions *i.e.* it is like two diodes. The junction between em and base may be called *emitter-base diode* or simply the *emitter diode*. The junction between base and collector may be called *collector-base diode* or simply *collector diode*.

(*iv*) The emitter diode is always forward biased whereas collector diode is always reverse ased.

(*v*) The resistance of emitter diode (forward biased) is very small as compared to colle diode (reverse biased). Therefore, forward bias applied to the emitter diode is generally very sm whereas reverse bias on the collector diode is much higher.

8.4 Transistor Action

The emitter-base junction of a transistor is forward biased whereas collector-base junction is reve biased. If for a moment, we ignore the presence of emitter-base junction, then *practically*[*] no curr would flow in the collector circuit because of the reverse bias. However, if the emitter-base junct is also present, then forward bias on it causes the emitter current to flow. It is seen that this emit current almost entirely flows in the collector circuit. Therefore, the current in the collector circ depends upon the emitter current. If the emitter current is zero, then collector current is nearly ze However, if the emitter current is 1mA, then collector current is also about 1mA. This is precise what happens in a transistor. We shall now discuss this transistor action for *npn* and *pnp* transisto

(*i*) **Working of npn transistor.** Fig. 8.4 shows the *npn* transistor with forward bias to emitte base junction and reverse bias to collector-base junction. The forward bias causes the electrons in th *n*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electro flow through the *p*-type base, they tend to combine with holes. As the base is lightly doped and ve thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base[**] current I_B The remainder ([***] more than 95%) cross over into the collector region to constitute collector curre I_C. In this way, almost the entire emitter current flows in the collector circuit. It is clear that emitte current is the sum of collector and base currents *i.e.*

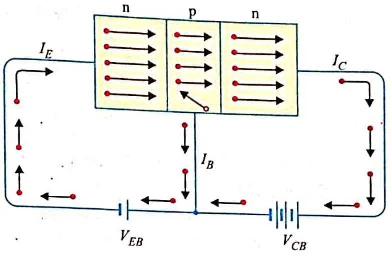
$$I_E = I_B + I_C$$

---

[*] In actual practice, a very little current (a few µA) would flow in the collector circuit. This is called collector cut off current and is due to minority carriers.

[**] The electrons which combine with holes become valence electrons. Then as valence electrons, they flow down through holes and into the external base lead. This constitutes base current I_B.

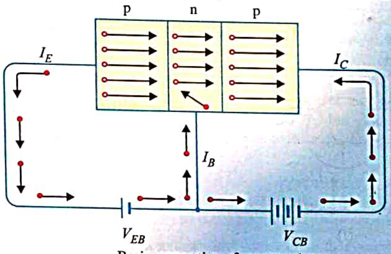
[***] The reasons that most of the electrons from emitter continue their journey through the base to collector to form collector current are : (*i*) The base is lightly doped and very thin. Therefore, there are a few holes which find enough time to combine with electrons. (*ii*) The reverse bias on collector is quite high and exerts attractive forces on these electrons.



Basic connection of *npn* transistor

Fig. 8.4

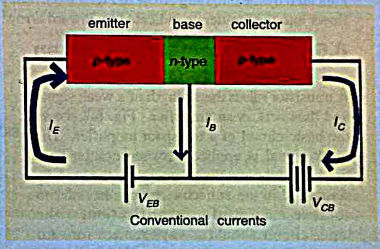
(*ii*) **Working of pnp transistor.** Fig. 8.5 shows the basic connection of a *pnp* transistor. The forward bias causes the holes in the *p*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes cross into *n*-type base, they tend to combine with the electrons. As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the electrons. The remainder (more than 95%) cross into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It may be noted that current conduction within *pnp* transistor is by holes. However, in the external connecting wires, the current is still by electrons.



Basic connection of *pnp* transistor

Fig. 8.5

Importance of transistor action. The input circuit (*i.e.* emitter-base junction) has low resistance because of forward bias whereas output circuit (*i.e.* collector-base junction) has high resistance due to reverse bias. As we have seen, the input emitter current almost entirely flows in the collector circuit. Therefore, a transistor transfers the input signal current from a low-resistance circuit to a high-resistance circuit. This is the key factor responsible for

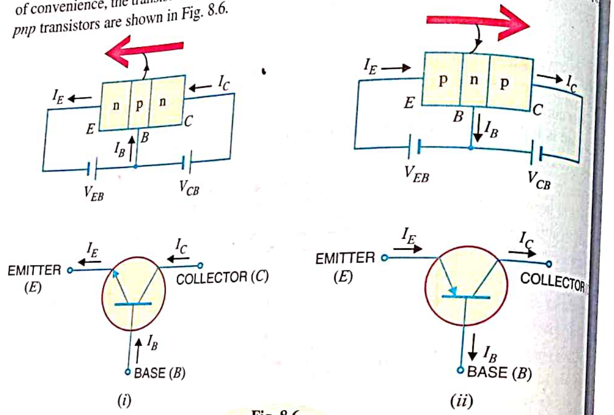


the amplifying capability of the transistor. We shall discuss the amplifying property of transis in this chapter.

Note. There are two basic transistor types : the **bipolar junction transistor (*BJT*)** and **effect transistor** (*FET*). As we shall see, these two transistor types differ in both their ope characteristics and their internal construction. **Note that when we use the term transistor, it** **bipolar junction transistor (*BJT*)**. The term comes from the fact that in a bipolar transistor, the *two* types of charge carriers (*viz.* electrons and holes) that play part in conductions. Note th means two and polar refers to polarities. The field-effect transistor is simply referred to as FET

8.5 Transistor Symbols

In the earlier diagrams, the transistors have been shown in diagrammatic form. However, for the of convenience, the transistors are represented by schematic diagrams. The symbols used for npn *pnp* transistors are shown in Fig. 8.6.



(*i*) (*ii*)

Fig. 8.6

Note that emitter is shown by an arrow which indicates the direction of conventional current fl with forward bias. For *npn* connection, it is clear that conventional current flows out of the emitter indicated by the outgoing arrow in Fig. 8.6 (*i*). Similarly, for *pnp* connection, the conventional curr flows into the emitter as indicated by inward arrow in Fig. 8.6 (*ii*).

8.6 Transistor Circuit as an Amplifier

A transistor raises the strength of a weak signal and thus acts as an amplifier. Fig. 8.7 shows the basic circuit of a transistor amplifier. The weak signal is applied between emitter-base junction and output is taken across the load R_C connected in the collector circuit. In order to achieve faithful amplification, the input circuit should always remain forward biased. To do so, a d.c. voltage V_{EE} is applied in the input circuit in addition to the signal as shown. This d.c. voltage is known as bias voltage and its magnitude is such that it always keeps the input circuit forward biased regardless of the polarity of the signal.

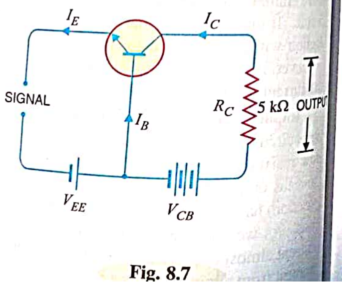


Fig. 8.7

As the input circuit has low resistance, therefore, a small change in signal voltage causes an appreciable change in emitter current. This causes almost the *same change in collector current due to transistor action. The collector current flowing through a high load resistance R_C produces a large voltage across it. Thus, a weak signal applied in the input circuit appears in the amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

How Amplifiers Work

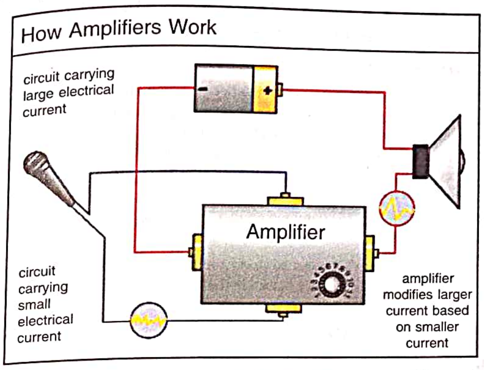


Illustration. The action of a transistor as an amplifier can be made more illustrative if we consider typical circuit values. Suppose collector load resistance R_C = 5 kΩ. Let us further assume that a change of 0.1 V in signal voltage produces a change of 1 mA in emitter current. Obviously, the change in collector current would also be approximately 1 mA. This collector current flowing through collector load R_C would produce a voltage = 5 kΩ × 1 mA = 5 V. Thus, a change of 0.1 V in the signal has caused a change of 5 V in the output circuit. In other words, the transistor has been able to raise the voltage level of the signal from 0.1 V to 5 V *i.e.* voltage amplification is 50.

Example 8.1. *A common base transistor amplifier has an input resistance of 20 Ω and output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume α_{ac} to be nearly one.*

Solution. **Fig. 8.8 shows the conditions of the problem. Note that output resistance is very high as compared to input resistance. This is not surprising because input junction (base to emitter) of the transistor is forward biased while the output junction (base to collector) is reverse biased.

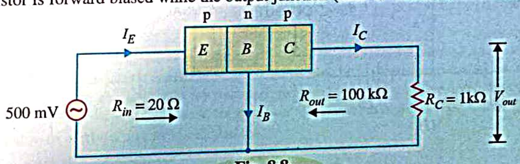


Fig. 8.8

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* The reason is as follows. The collector-base junction is reverse biased and has a very high resistance of the order of mega ohms. Thus collector-base voltage has little effect on the collector current. This means that a large resistance R_C can be inserted in series with collector without disturbing the collector current relation to the emitter current *viz.* $I_C = \alpha I_E + I_{CBO}$. Therefore, collector current variations caused by a small base-emitter voltage fluctuations result in voltage changes in R_C that are quite high—often hundreds of times larger than the emitter-base voltage.

** The d.c. biasing is omitted in the figure because our interest is limited to amplification.

Input current, $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500\text{ mV}}{20\ \Omega} = 25\text{ mA}$. Since α_{ac} is nearly 1, output current 25 mA.

$$\text{Output voltage, } V_{out} = I_C R_C = 25\text{ mA} \times 1\text{ k}\Omega = 25\text{ V}$$

$$\therefore \quad \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25\ V}{500\ mV} = \mathbf{50}$$

Comments. The reader may note that basic amplifying action is produced by tra current from a *low-resistance* to a *high-resistance* circuit. Consequently, the name transist to the device by combining the two terms given in magenta letters below :

Transfer + Res**istor** ⟶ **Transistor**

8.7 Transistor Connections

There are three leads in a transistor *viz.*, emitter, base and collector terminals. However transistor is to be connected in a circuit, we require four terminals; two for the input and t output. This difficulty is overcome by making one terminal of the transistor common to b and output terminals. The input is fed between this common terminal and one of the o terminals. The output is obtained between the common terminal and the remaining terminal ingly; a transistor can be connected in a circuit in the following three ways :

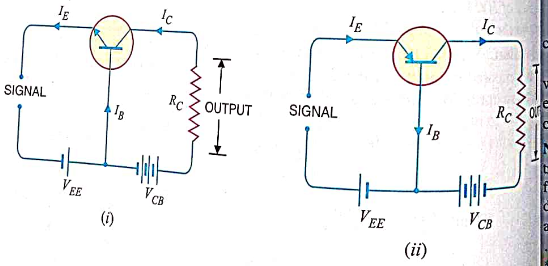
(*i*) common base connection (*ii*) common emitter connection

(*iii*) common collector connection

Each circuit connection has specific advantages and disadvantages. It may be noted regardless of circuit connection, the emitter is always biased in the forward direction, whil lector always has a reverse bias.

8.8 Common Base Connection

In this circuit arrangement, input is applied between emitter and base and output is taken from tor and base. Here, base of the transistor is common to both input and output circuits and h name common base connection. In Fig. 8.9 (*i*), a common base *npn* transistor circuit is shown Fig. 8.9 (*ii*) shows the common base *pnp* transistor circuit.



(*i*) (*ii*)

Fig. 8.9

1. **Current amplification factor (α).** It is the ratio of output current to input current common base connection, the input current is the emitter current I_E and output current is the col current I_C.

The ratio of change in collector current to the change in emitter current at constant col base voltage V_{CB} *is known as* **current amplification factor** *i.e.*

$$^*\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

It is clear that current amplification factor is less than **unity. This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base thin and doping it lightly. Practical values of α in commercial transistors range from 0.9 to 0.99.

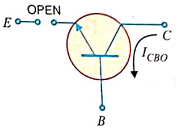


Fig. 8.10

2. **Expression for collector current.** The whole of emitter current does not reach the collector. It is because a small percentage of it, as a result of electron-hole combinations occurring in base area, gives rise to base current. Moreover, as the collector-base junction is reverse biased, therefore, some leakage current flows due to minority carriers. It follows, therefore, that total collector current consists of :

(*i*) That part of emitter current which reaches the collector terminal *i.e.* ***αI_E.

(*ii*) The leakage current $I_{leakage}$. This current is due to the movement of minority carriers across base-collector junction on account of it being reverse biased. This is generally much smaller than αI_E.

$$\therefore \quad \text{Total collector current, } I_C = \alpha I_E + I_{leakage}$$

It is clear that if $I_E = 0$ (*i.e.*, emitter circuit is open), a small leakage current still flows in the collector circuit. This $I_{leakage}$ is abbreviated as I_{CBO}, meaning collector-base current with emitter open. The I_{CBO} is indicated in Fig. 8.10.

$$\therefore \quad I_C = \alpha I_E + I_{CBO} \quad \text{...}(i)$$

$$\text{Now} \quad I_E = I_C + I_B$$

$$\therefore \quad I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$\text{or} \quad I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$\text{or} \quad I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} \quad \text{...}(ii)$$

Relation (*i*) or (*ii*) can be used to find I_C. It is further clear from these relations that the collector current of a transistor can be controlled by either the emitter or base current.

Fig. 8.11 shows the concept of I_{CBO}. In *CB* configuration, a small collector current flows even when the emitter current is zero. This is the leakage collector current (*i.e.* the collector current when emitter is open) and is denoted by I_{CBO}. When the emitter voltage V_{EE} is also applied, the various currents are as shown in Fig. 8.11 (*ii*).

Note. Owing to improved construction techniques, the magnitude of I_{CBO} for general-purpose and low-powered transistors (especially silicon transistors) is usually very small and may be neglected in calculations. However, for high power applications, it will appear in microampere range. Further, I_{CBO} is very much temperature dependent; it increases rapidly with the increase in temperature. Therefore, at higher temperatures, I_{CBO} plays an important role and must be taken care of in calculations.

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[*] If only d.c. values are considered, then $\alpha = I_C/I_E$.

[**] At first sight, it might seem that since there is no current gain, no voltage or power amplification could be possible with this arrangement. However, it may be recalled that output circuit resistance is much higher than the input circuit resistance. Therefore, it does give rise to voltage and power gain.

[***] $$\alpha = \frac{I_C}{I_E} \quad \therefore \quad I_C = \alpha I_E$$

In other words, αI_E part of emitter current reaches the collector terminal.

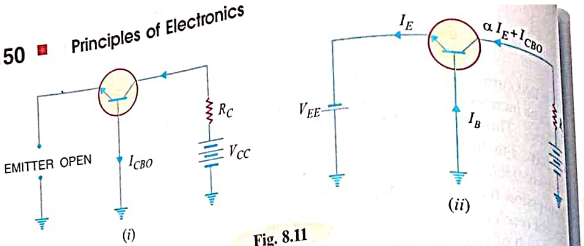

Fig. 8.11

Example 8.2. *In a common base connection, $I_E = 1mA$, $I_C = 0.95mA$. Calculate the value*

Solution. Using the relation, $I_E = I_B + I_C$

$1 = I_B + 0.95$

or $I_B = 1 - 0.95 =$ **0.05 mA**

∴

Example 8.3. *In a common base connection, current amplification factor is 0.9. If the em current is 1mA, determine the value of base current.*

Solution. Here, $\alpha = 0.9, \quad I_E = 1$ mA

Now $\alpha = \frac{I_C}{I_E}$

or $I_C = \alpha I_E = 0.9 \times 1 = 0.9$ mA

Also $I_E = I_B + I_C$

∴ Base current, $I_B = I_E - I_C = 1 - 0.9 =$ **0.1 mA**

Example 8.4. *In a common base connection, $I_C = 0.95$ mA and $I_B = 0.05$ mA. Find the v of α.*

Solution. We know $I_E = I_B + I_C = 0.05 + 0.95 = 1$ mA

∴ Current amplification factor, $\alpha = \frac{I_C}{I_E} = \frac{0.95}{1} =$ **0.95**

Example 8.5. *In a common base connection, the emitter current is 1mA. If the emitter circu open, the collector current is 50 μA. Find the total collector current. Given that α = 0.92.*

Solution. Here, $I_E = 1$ mA, $\alpha = 0.92, \quad I_{CBO} = 50$ μA

∴ Total collector current, $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$

$= 0.92 + 0.05 =$ **0.97 mA**

Example 8.6. *In a common base connection, α = 0.95. The voltage drop across 2 kΩ resistan which is connected in the collector is 2V. Find the base current.*

Solution. Fig. 8.12 shows the required common base connection. The voltage drop across R_C 2 kΩ) is 2V.

∴

Now $I_C = 2\text{ V}/2\text{ k}\Omega = 1$ mA

$\alpha = I_C/I_E$

∴ $I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05$ mA

Using the relation, $I_E = I_B + I_C$

∴ $I_B = I_E - I_C = 1.05 - 1$

$=$ **0.05 mA**

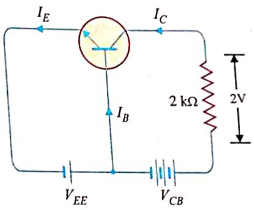

Fig. 8.12

Example 8.7. *For the common base circuit shown in Fig. 8.13, determine I_C and V_{CB}. Assume the transistor to be of silicon.*

Solution. Since the transistor is of silicon, $V_{BE} = 0.7$V. Applying Kirchhoff's voltage law to the emitter-side loop, we get,

$V_{EE} = I_E R_E + V_{BE}$

or $I_E = \frac{V_{EE} - V_{BE}}{R_E}$

$= \frac{8V - 0.7V}{1.5\text{ k}\Omega} = 4.87$ mA

∴ $I_C \simeq I_E =$ **4.87 mA**

Applying Kirchhoff's voltage law to the collector-side loop, we have,

$V_{CC} = I_C R_C + V_{CB}$

∴ $V_{CB} = V_{CC} - I_C R_C$

$= 18\text{ V} - 4.87\text{ mA} \times 1.2\text{ k}\Omega =$ **12.16 V**

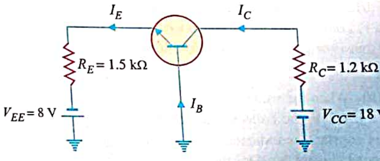

Fig. 8.13

8.9 Characteristics of Common Base Connection

The complete electrical behaviour of a transistor can be described by stating the interrelation of the various currents and voltages. These relationships can be conveniently displayed graphically and the curves thus obtained are known as the characteristics of transistor. The most important characteristics of common base connection are *input characteristics* and *output characteristics.*

1. Input characteristic. It is the curve between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The emitter current is generally taken along *y*-axis and emitter-base voltage along *x*-axis. Fig. 8.14 shows the input characteristics of a typical transistor in *CB* arrangement . The following points may be noted from these characteristics :

(*i*) The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.

(*ii*) The emitter current is almost independent of collector-base voltage V_{CB}. This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.

Input resistance. It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting

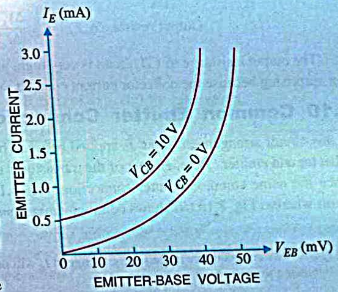

Fig. 8.14

change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) *i.e.*

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_E} \text{ at constant } V_{CB}$$

In fact, input resistance is the opposition offered to the signal current. As a very small sufficient to produce a large flow of emitter current I_E, therefore, input resistance is quite small, order of a few ohms.

2. **Output characteristic.** It is the curve between collector current I_C and collector-base age V_{CB} at *constant emitter current I_E. Generally, collector current is taken along *y*-axis and tor-base voltage along *x*-axis. Fig. 8.15 shows the output characteristics of a typical transistor arrangement.

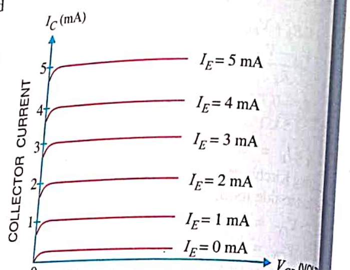

Fig. 8.15

The following points may be noted from the characteristics :

(*i*) The collector current I_C varies with V_{CB} only at very low voltages ($<$ 1V). The transistor is *never* operated in this region.

(*ii*) When the value of V_{CB} is raised above 1 – 2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon I_E only. This is consistent with the theory that the emitter current flows *almost* entirely to the collector terminal. The transistor is *always* operated in this region.

(*iii*) A very large change in collector-base voltage produces only a tiny change in collector current. This means that output resistance is very high.

Output resistance. It is the ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

The output resistance of *CB* circuit is very high, of the order of several tens of kilo-ohms. This is not surprising because the collector current changes very slightly with the change in V_{CB}.

8.10 Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter. Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter connection. Fig. 8.16 (*i*) shows common emitter *npn* transistor circuit whereas Fig. 8.16 (*ii*) shows common emitter *pnp* transistor circuit.

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[*] I_E has to be kept constant because any change in I_E will produce corresponding change in I_C. Here, we are interested to see how V_{CB} influences I_C.

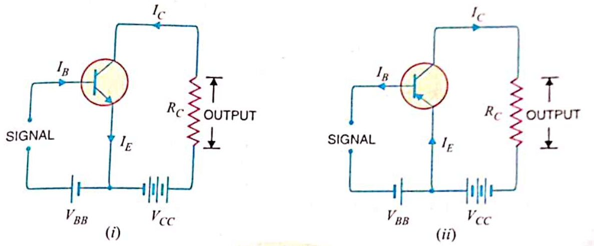


Fig. 8.16

1. **Base current amplification factor (β).** In common emitter connection, input current is I_B and output current is I_C.

The ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) is known as **base current amplification factor** *i.e.*

$$\beta^* = \frac{\Delta I_C}{\Delta I_B}$$

In almost any transistor, less than 5% of emitter current flows as the base current. Therefore, the value of β is generally greater than 20. Usually, its value ranges from 20 to 500. This type of connection is frequently used as it gives appreciable current gain as well as voltage gain.

Relation between β and α. A simple relation exists between β and α. This can be derived as follows :

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{...}(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{...}(ii)$$

Now $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \quad \text{...}(iii)$$

Dividing the numerator and denominator of R.H.S. of exp. (*iii*) by ΔI_E, we get,

$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha} \qquad \left[\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right]$$

$$\therefore \quad \beta = \frac{\alpha}{1-\alpha}$$

It is clear that as α approaches unity, β approaches infinity. In other words, the current gain in common emitter connection is very high. It is due to this reason that this circuit arrangement is used in about 90 to 95 percent of all transistor applications.

---

[*] If d.c. values are considered, $\beta = I_C/I_B$.

2. Expression for collector current. In common emitter circuit, I_B is the input current is the output current.

We know $I_E = I_B + I_C$

and $I_C = \alpha I_E + I_{CBO}$

From exp. (*ii*), we get, $I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$

or $I_C (1 - \alpha) = \alpha I_B + I_{CBO}$

or $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

From exp. (*iii*), it is apparent that if $I_B = 0$ (*i.e.* base circuit is open), the collector current the current to the emitter. This is abbreviated as I_{CEO}, meaning collector-emitter current with base

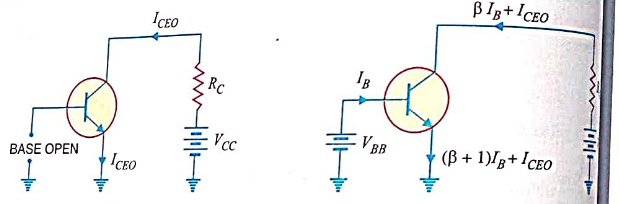
$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

∴ Substituting the value of $\frac{1}{1-\alpha} I_{CBO} = I_{CEO}$ in exp. (*iii*), we get,

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

or $$I_C = \beta I_B + I_{CEO} \qquad (\because \beta =$$

Concept of I_{CEO}. In *CE* configuration, a small collector current flows even when the current is zero [See Fig. 8.17 (*i*)]. This is the collector cut off current (*i.e.* the collector current flows when base is open) and is denoted by I_{CEO}. The value of I_{CEO} is much larger than I_{CBO}.



(*i*) (*ii*)

Fig. 8.17

When the base voltage is applied as shown in Fig. 8.17 (*ii*), then the various currents are:

Base current $= I_B$

Collector current $= \beta I_B + I_{CEO}$

Emitter current $=$ Collector current + Base current

$= (\beta I_B + I_{CEO}) + I_B = (\beta + 1) I_B + I_{CEO}$

It may be noted here that :

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO} = (\beta + 1) I_{CBO} \qquad \left[\because \frac{1}{1-\alpha} = \beta\right.$$

8.11. Measurement of Leakage Current

A very small leakage current flows in all transistor circuits. However, in most cases, it is quite and can be neglected.

(*i*) **Circuit for I_{CEO} test.** Fig. 8.18 shows the circuit for measuring I_{CEO}. Since base is

($I_B = 0$), the transistor is in cut off. Ideally, $I_C = 0$ but actually there is a small current from collector to emitter due to minority carriers. It is called I_{CEO} (collector-to-emitter current with base open). This current is usually in the nA range for silicon. A faulty transistor will often have excessive leakage current.

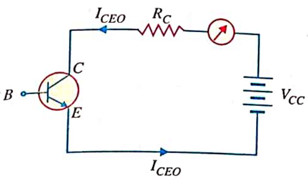


Fig. 8.18

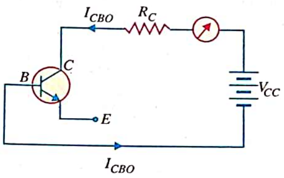


Fig. 8.19

(*ii*) **Circuit for I_{CBO} test.** Fig. 8.19 shows the circuit for measuring I_{CBO}. Since the emitter is open ($I_E = 0$), there is a small current from collector to base. This is called I_{CBO} (collector-to-base current with emitter open). This current is due to the movement of minority carriers across base-collector junction. The value of I_{CBO} is also small. If in measurement, I_{CBO} is excessive, then there is a possibility that collector-base is shorted.

Example 8.8. *Find the value of β if (i) α = 0.9 (ii) α = 0.98 (iii) α = 0.99.*

Solution. (*i*) $\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = \mathbf{9}$

(*ii*) $\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \mathbf{49}$

(*iii*) $\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = \mathbf{99}$

Example 8.9. *Calculate I_E in a transistor for which β = 50 and I_B = 20 μA.*

Solution. Here $\beta = 50$, $I_B = 20\mu A = 0.02$ mA

Now $\beta = \frac{I_C}{I_B}$

∴ $I_C = \beta I_B = 50 \times 0.02 = 1$ mA

Using the relation, $I_E = I_B + I_C = 0.02 + 1 = \mathbf{1.02\ mA}$

Example 8.10. *Find the α rating of the transistor shown in Fig. 8.20. Hence determine the value of I_C using both α and β rating of the transistor.*

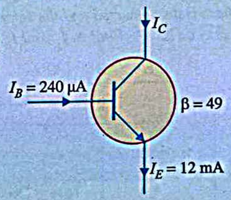


Fig. 8.20

Solution. Fig. 8.20 shows the conditions of the problem.

$$\alpha = \frac{\beta}{1+\beta} = \frac{49}{1+49} = \mathbf{0.98}$$

The value of I_C can be found by using either α or β rating as under :

$I_C = \alpha I_E = 0.98$ (12 mA) $=$ **11.76 mA**

Also $I_C = \beta . I_B = 49$ (240 μA) $=$ **11.76 mA**

Example 8.11. *For a transistor, $\beta = 45$ and voltage drop across 1kΩ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.*

Solution. Fig. 8.21 shows the required common emitter connection. The voltage drop across R_C (= 1 kΩ) is 1volt.

$$\therefore \quad I_C = \frac{1\,V}{1\,k\Omega} = 1\text{ mA}$$

$$\text{Now} \quad \beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{1}{45} = \mathbf{0.022\ mA}$$

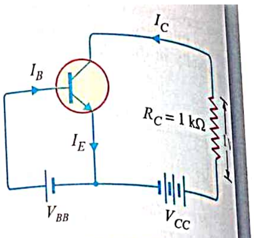


Fig. 8.21

Example 8.12. *A transistor is connected in common emitter (CE) configuration in which collector supply is 8V and the voltage drop across resistance R_C connected in the collector circuit is 0.5V. The value of $R_C = 800\ \Omega$. If $\alpha = 0.96$, determine :*

(i) collector-emitter voltage

(ii) base current

Solution. Fig. 8.22 shows the required common emitter connection with various values.

(*i*) Collector-emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = \mathbf{7.5\ V}$$

(*ii*) The voltage drop across R_C (= 800 Ω) is 0.5 V.

$$\therefore \quad I_C = \frac{0.5\text{ V}}{800\ \Omega} = \frac{5}{8}\text{ mA} = 0.625\text{ mA}$$

$$\text{Now} \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24$$

$$\therefore \text{ Base current, } I_B = \frac{I_C}{\beta} = \frac{0.625}{24} = \mathbf{0.026\ mA}$$

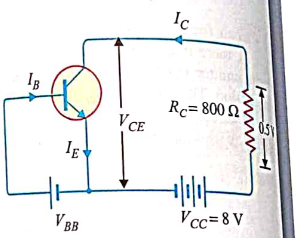
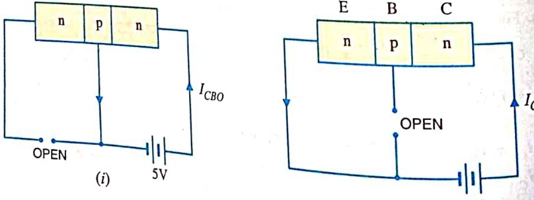


Fig. 8.22

Example 8.13. *An n-p-n transistor at room temperature has its emitter disconnected. A voltag of 5V is applied between collector and base. With collector positive, a current of 0.2 µA flows. Whe the base is disconnected and the same voltage is applied between collector and emitter, the current i found to be 20 µA. Find α, I_E and I_B when collector current is 1mA.*



(*i*)

(*ii*)

Fig. 8.23

Solution. When the emitter circuit is open [See Fig. 8.23 (*i*)], the collector-base junction is reverse biased. A small leakage current I_{CBO} flows due to minority carriers.

$$\therefore \quad I_{CBO} = 0.2\ \mu A \qquad \text{...given}$$

When base is open [See Fig. 8.23 (*ii*)], a small leakage current I_{CEO} flows due to minority carriers.

$$\therefore \quad I_{CEO} = 20\ \mu A \qquad \text{. . . given}$$

$$\text{We know} \quad I_{CEO} = \frac{I_{CBO}}{1-\alpha}$$

$$\text{or} \quad 20 = \frac{0.2}{1-\alpha}$$

$$\therefore \quad \alpha = \mathbf{0.99}$$

$$\text{Now} \quad I_C = \alpha I_E + I_{CBO}$$

$$\text{Here} \quad I_C = 1\text{mA} = 1000\ \mu A\ ;\ \alpha = 0.99\ ;\ I_{CBO} = 0.2\ \mu A$$

$$\therefore \quad 1000 = 0.99 \times I_E + 0.2$$

$$\text{or} \quad I_E = \frac{1000 - 0.2}{0.99} = \mathbf{1010\ \mu A}$$

$$\text{and} \quad I_B = I_E - I_C = 1010 - 1000 = \mathbf{10\ \mu A}$$

Example 8.14. *The collector leakage current in a transistor is 300 µA in CE arrangement. If now the transistor is connected in CB arrangement, what will be the leakage current? Given that $\beta = 120$.*

Solution. $I_{CEO} = 300\ \mu A$

$$\beta = 120\ ;\ \alpha = \frac{\beta}{\beta+1} = \frac{120}{120+1} = 0.992$$

$$\text{Now,} \quad I_{CEO} = \frac{I_{CBO}}{1-\alpha}$$

$$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.992) \times 300 = \mathbf{2.4\ \mu A}$$

Note that leakage current in *CE* arrangement (*i.e.* I_{CEO}) is much more than in *CB* arrangement (*i.e.* I_{CBO}).

Example 8.15. *For a certain transistor, $I_B = 20\ \mu A$; $I_C = 2$ mA and $\beta = 80$. Calculate I_{CBO}.*

Solution.

$$I_C = \beta I_B + I_{CEO}$$

$$\text{or} \quad 2 = 80 \times 0.02 + I_{CEO}$$

$$\therefore \quad I_{CEO} = 2 - 80 \times 0.02 = 0.4\text{ mA}$$

$$\text{Now} \quad \alpha = \frac{\beta}{\beta+1} = \frac{80}{80+1} = 0.988$$

$$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.988) \times 0.4 = \mathbf{0.0048\ mA}$$

Example 8.16. *Using diagrams, explain the correctness of the relation $I_{CEO} = (\beta + 1)\, I_{CBO}$.*

Solution. The leakage current I_{CBO} is the current that flows through the base-collector junction when emitter is open as shown is Fig. 8.24. When the transistor is in *CE* arrangement, the *base current (*i.e.* I_{CBO}) is multiplied by β in the collector as shown in Fig. 8.25.

$$\therefore \quad I_{CEO} = I_{CBO} + \beta I_{CBO} = (\beta + 1)\, I_{CBO}$$

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* The current I_{CBO} is amplified because it is forced to flow across the base-emitter junction.

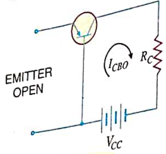


Fig. 8.24

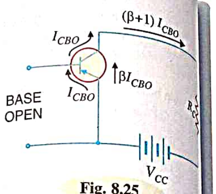
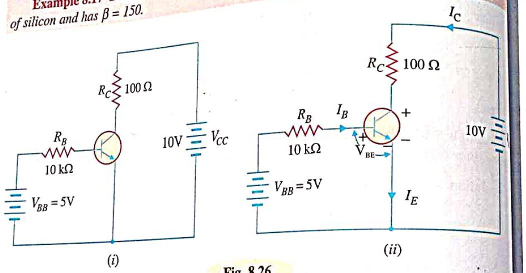


Fig. 8.25

Example 8.17 *Determine V_{CB} in the transistor* circuit shown in Fig. 8.26 (i). The transis of silicon and has $\beta = 150$.*



(i) (ii)

Fig. 8.26

Solution. Fig. 8.26 (*i*) shows the transistor circuit while Fig. 8.26 (*ii*) shows the various curre and voltages along with polarities.

Applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or $$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{10\ k\Omega} = 430\ \mu A$$

∴ $$I_C = \beta I_B = (150)(430\ \mu A) = 64.5\ mA$$

Now $$V_{CE} = V_{CC} - I_C R_C$$

$$= 10V - (64.5\ mA)\ (100\Omega) = 10V - 6.45V = 3.55V$$

We know that : $$V_{CE} = V_{CB} + V_{BE}$$

∴ $$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = \mathbf{2.85V}$$

Example 8.18. *In a transistor, $I_B = 68\ \mu A$, $I_E = 30\ mA$ and $\beta = 440$. Determine the α rating the transistor. Then determine the value of I_C using both the α rating and β rating of the transis*

Solution.

$$\alpha = \frac{\beta}{\beta+1} = \frac{440}{440+1} = \mathbf{0.9977}$$

---

* The resistor R_B controls the base current I_B and hence collector current I_C (= βI_B). If R_B is increased, t base current (I_B) decreases and hence collector current (I_C) will decrease and vice-versa.

$$I_C = \alpha I_E = (0.9977)\ (30\ mA) = \mathbf{29.93\ mA}$$

Also $$I_C = \beta I_B = (440)\ (68\ \mu A) = \mathbf{29.93\ mA}$$

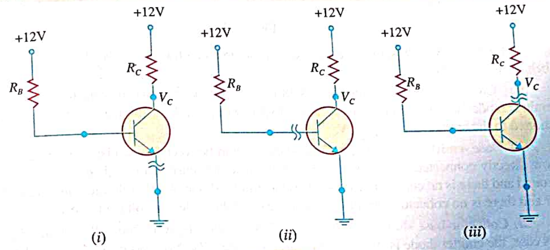
Example 8.19. *A transistor has the following ratings : $I_{C\ (max)} = 500$ mA and $\beta_{max} = 300$. Determine the maximum allowable value of I_B for the device.*

Solution.

$$I_{B\ (max)} = \frac{I_{C\ (max)}}{\beta_{max}} = \frac{500\ mA}{300} = \mathbf{1.67\ mA}$$

For this transistor, if the base current is allowed to exceed 1.67 mA, the collector current will exceed its maximum rating of 500 mA and the transistor will probably be destroyed.

Example 8.20. *Fig. 8.27 shows the open circuit failures in a transistor. What will be the circuit behaviour in each case ?*



(i) (ii) (iii)

Fig. 8.27

Solution. Fig 8.27 shows the open circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) **Open emitter.** Fig. 8.27 (*i*) shows an open emitter failure in a transistor. Since the collector diode is not forward biased, it is *OFF* and there can be neither collector current nor base current. Therefore, there will be no voltage drops across either resistor and the voltage at the base and at the collector leads of the transistor will be 12V.

(*ii*) **Open-base.** Fig. 8.27 (*ii*) shows an open base failure in a transistor. Since the base is open, there can be no base current so that the transistor is in *cut-off*. Therefore, all the transistor currents are 0A. In this case, the base and collector voltages will both be at 12V.

Note. It may be noted that an open failure at either the base or emitter will produce similar results.

(*iii*) **Open collector.** Fig. 8.27 (*iii*) shows an open collector failure in a transistor. In this case, the emitter diode is still *ON*, so we expect to see 0.7V at the base. However, we will see 12V at the collector because there is no collector current.

Example 8.21. *Fig. 8.28 shows the short circuit failures in a transistor. What will be the circuit behaviour in each case ?*

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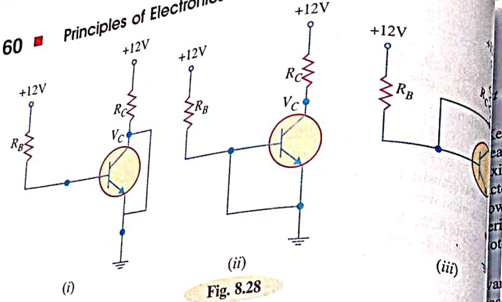
* The collector resistor R_C controls the collector voltage $V_C (= V_{CC} - I_C R_C)$. When R_C increases, V_C decreases and vice-versa.



(i) (ii) (iii)

Fig. 8.28

Solution. Fig. 8.28 shows the short circuit failures in a transistor. We shall discuss th behaviour in each case.

(i) **Collector-emitter short.** Fig. 8.28 (i) shows a short between collector and em emitter diode is still forward biased, so we expect to see 0.7V at the base. Since the col shorted to the emitter, $V_C = V_E = 0V$.

(ii) **Base -emitter short.** Fig 8.28 (ii) shows a short between base and emitter. Since th now directly connected to ground, $V_B = 0$. Therefore, the current through R_B will be dir ground and there is no current to forward bias the emitter diode. As a result, the transistor wil *off* and there is no collector current. So we will expect the collector voltage to be 12V.

(iii) **Collector-base short.** Fig. 8.28 (iii) shows a short between the collector and the this case, the emitter diode is still forward biased so $V_B = 0.7V$. Now, however, because the c is shorted to the base, $V_C = V_B = 0.7V$.

Note. The collector-emitter short is probably the most common type of fault in a transis because the collector current (I_C) and collector-emitter voltage (V_{CE}) are responsible for th part of the power dissipation in the transistor. As we shall see (See Art. 8.23), the power dissip a transistor is mainly due to I_C and V_{CE} (*i.e.* $P_D = V_{CE}\, I_C$). Therefore, the transistor chip betw collector and the emitter is most likely to melt first.

8.12 Characteristics of Common Emitter Connection

The important characteristics of this circuit arrangement are the *input characteristics* and *characteristics*.

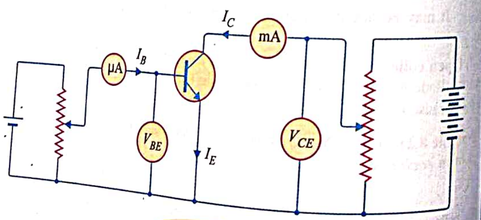


Fig. 8.29

1. **Input characteristic.** *It is the curve between base current I_B and base-emitter voltage V_{BE} constant collector-emitter voltage V_{CE}.*

The input characteristics of a *CE* connection can be determined by the circuit shown in Fig. 8.29. eeping V_{CE} constant (say at 10 V), note the base current I_B for various values of V_{BE}. Then plot the eadings obtained on the graph, taking I_B along *y*-xis and V_{BE} along *x*-axis. This gives the input charcteristic at V_{CE} = 10V as shown in Fig. 8.30. Folowing a similar procedure, a family of input characeristics can be drawn. The following points may be oted from the characteristics :

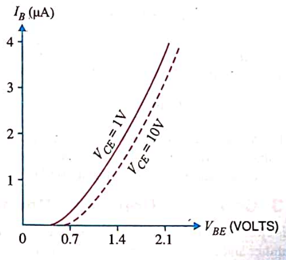


Fig. 8.30

(i) The characteristic resembles that of a forard biased diode curve. This is expected since the ase-emitter section of transistor is a diode and it is orward biased.

(ii) As compared to *CB* arrangement, I_B ncreases less rapidly with V_{BE}. Therefore, input esistance of a *CE* circuit is higher than that of *CB* ircuit.

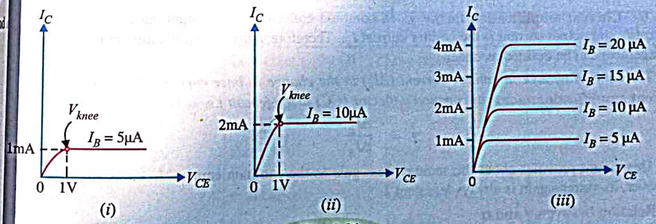
Input resistance. It is the ratio of change in ase-emitter voltage (ΔV_{BE}) to the change in base urrent (ΔI_B) at constant V_{CE} *i.e.*

$$\text{Input resistance,} \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{at constant } V_{CE}$$

The value of input resistance for a *CE* circuit is of the order of a few hundred ohms.

2. **Output characteristic.** *It is the curve between collector current I_C and collector-emitter oltage V_{CE} at constant base current I_B.*

The output characteristics of a *CE* circuit can be drawn with the help of the circuit shown in Fig. .29. Keeping the base current I_B fixed at some value say, 5 μA, note the collector current I_C for arious values of V_{CE}. Then plot the readings on a graph, taking I_C along *y*-axis and V_{CE} along *x*-axis. his gives the output characteristic at I_B = 5 μA as shown in Fig. 8.31 (*i*). The test can be repeated for I_B = 10 μA to obtain the new output characteristic as shown in Fig. 8.31 (*ii*). Following similar rocedure, a family of output characteristics can be drawn as shown in Fig. 8.31 (*iii*).



(i) (ii) (iii)

Fig. 8.31

The following points may be noted from the characteristics:

(i) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, collector urrent becomes *almost* constant and independent of V_{CE}. This value of V_{CE} upto which collector

current I_C changes with V_{CE} is called the *knee voltage* (V_{knee}). *The transistors are always operat*
the region above knee voltage.

(ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with incre
V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority c
ers before electron-hole combinations occur in the base area.

(iii) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equ
$\beta \times I_B$.

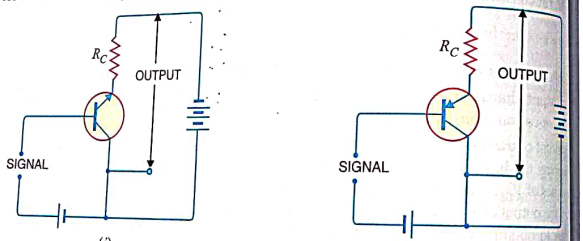
Output resistance. It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the chang
collector current (ΔI_C) at constant I_B *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

It may be noted that whereas the output characteristics of *CB* circuit are horizontal, they h
noticeable slope for the *CE* circuit. Therefore, the output resistance of a *CE* circuit is less than the
CB circuit. Its value is of the order of 50 kΩ.

8.13 Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken betw
the emitter and collector. Here, collector of the transistor is common to both input and output circu
and hence the name common collector connection. Fig. 8.32 (*i*) shows common collector *npn* tran
tor circuit whereas Fig. 8.32 (*ii*) shows common collector *pnp* circuit.



(*i*) (*ii*)

Fig. 8.32

(*i*) **Current amplification factor γ.** In common collector circuit, input current is the bas
current I_B and output current is the emitter current I_E. Therefore, current amplification in this circu
arrangement can be defined as under :

The ratio of change in emitter current (ΔI_E) *to the change in base current* (ΔI_B) *is known a*
current amplification factor *in common collector (CC) arrangement i.e.*

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

This circuit provides about the same current gain as the common emitter circuit as $\Delta I_E \simeq \Delta I$
However, its voltage gain is always less than 1.

Relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \quad \ldots(i$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \ldots(ii$$

Now $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator of R.H.S. by ΔI_E, we get,

$$\gamma = \frac{\dfrac{\Delta I_E}{\Delta I_E}}{\dfrac{\Delta I_E}{\Delta I_E} - \dfrac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \qquad \left(\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right)$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha}$$

(*ii*) **Expression for collector current**

We know $I_C = \alpha I_E + I_{CBO}$ (See Art. 8.8)

Also $I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$

$\therefore$ $I_E(1-\alpha) = I_B + I_{CBO}$

or $I_E = \dfrac{I_B}{1-\alpha} + \dfrac{I_{CBO}}{1-\alpha}$

or $I_C \simeq I_E = {}^*(\beta+1)\,I_B + (\beta+1)\,I_{CBO}$

(*iii*) **Applications.** The common collector circuit has very high input resistance (about 750 kΩ) and very low output resistance (about 25 Ω). Due to this reason, the voltage gain provided by this circuit is always less than 1. Therefore, this circuit arrangement is seldom used for amplification. However, due to relatively high input resistance and low output resistance, this circuit is primarily used for impedance matching *i.e.* for driving a low impedance load from a high impedance source.

8.14 Comparison of Transistor Connections

The comparison of various characteristics of the three connections is given below in the tabular form.

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

The following points are worth noting about transistor arrangements :

---

* $\beta = \dfrac{\alpha}{1-\alpha} \quad \therefore \quad \beta + 1 = \dfrac{\alpha}{1-\alpha} + 1 = \dfrac{1}{1-\alpha}$

(i) **CB Circuit.** The input resistance (r_i) of CB circuit is low because I_E is high. The output resistance (r_o) is high because of reverse voltage at the collector. It has no current gain ($\alpha < 1$) but voltage gain can be high. The CB circuit is seldom used. The only advantage of CB circuit is that it provides good stability against increase in temperature.

(ii) **CE Circuit.** The input resistance (r_i) of a CE circuit is high because of small I_B. Therefore, r_i for a CE circuit is much higher than that of CB circuit. The output resistance (r_o) of CE circuit is smaller than that of CB circuit. The current gain of CE circuit is large because I_C is much larger than I_B. The voltage gain of CE circuit is larger than that of CB circuit. The CE circuit is generally used because it has the best combination of voltage gain and current gain. The disadvantage of CE circuit is that the leakage current is amplified in the circuit, but bias stabilisation methods can be used.

(iii) **CC Circuit.** The input resistance (r_i) and output resistance (r_o) of CC circuit are respectively high and low as compared to other circuits. There is no voltage gain ($A_v < 1$) in a CC circuit. This circuit is often used for impedance matching.

8.15 Commonly Used Transistor Connection

Out of the three transistor connections, the common emitter circuit is the most efficient. It is used in about 90 to 95 per cent of all transistor applications. The main reasons for the widespread use of this circuit arrangement are :

(i) **High current gain.** In a common emitter connection, I_C is the output current and I_B is the input current. In this circuit arrangement, collector current is given by :

$$I_C = \beta I_B + I_{CEO}$$

As the value of β is very large, therefore, the output current I_C is much more than the input current I_B. Hence, the current gain in CE arrangement is very high. It may range from 20 to 500.

(ii) **High voltage and power gain.** Due to high current gain, the common emitter circuit has the highest voltage and power gain of three transistor connections. This is the major reason for using the transistor in this circuit arrangement.

(iii) **Moderate output to input impedance ratio.** In a common emitter circuit, the ratio of output impedance to input impedance is small (about 50). This makes this circuit arrangement an ideal one for coupling between various transistor stages. However, in other connections, the ratio of output impedance to input impedance is very large and hence coupling becomes highly inefficient due to gross mismatching.

8.16 Transistor as an Amplifier in *CE* Arrangement

Fig. 8.33 shows the common emitter *npn* amplifier circuit. Note that a battery V_{BB} is connected in the input circuit in addition to the signal voltage. This d.c. voltage is known as *bias voltage* and its magnitude is such that it always keeps the emitter-base junction forward *biased regardless of the polarity of the signal source.

Operation. During the positive half-cycle of the **signal, the forward bias across the emitter-base junction is increased. Therefore, more electrons flow from the emitter to the collector *via* the base. This causes an increase in collector current. The increased collector current produces a greater voltage drop across the collector load resistance R_C. However, during the negative half-cycle of the signal, the forward bias across emitter-base junction is decreased. Therefore, collector current decreases. This results in the decreased output voltage (in the opposite direction). Hence, an amplified output is obtained across the load.

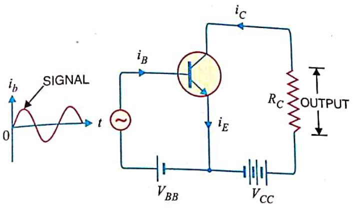


Fig. 8.33

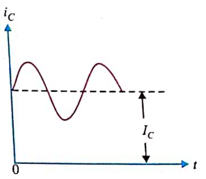


Fig. 8.34

Analysis of collector currents. When no signal is applied, the input circuit is forward biased by the battery V_{BB}. Therefore, a d.c. collector current I_C flows in the collector circuit. This is called *zero signal collector current*. When the signal voltage is applied, the forward bias on the emitter-base junction increases or decreases depending upon whether the signal is positive or negative. During the positive half-cycle of the signal, the forward bias on emitter-base junction is increased, causing total collector current i_C to increase. Reverse will happen for the negative half-cycle of the signal.

Fig. 8.34 shows the graph of total collector current i_C versus time. From the graph, it is clear that total collector current consists of two components, namely ;

(i) The d.c. collector current I_C (zero signal collector current) due to bias battery V_{BB}. This is the current that flows in the collector in the absence of signal.

(ii) The a.c. collector current i_c due to signal.

∴ Total collector current, $i_C = i_c + I_C$

The useful output is the voltage drop across collector load R_C due to the a.c. component i_c. The purpose of zero signal collector current is to ensure that the emitter-base junction is forward biased at all times. The table below gives the symbols usually employed for currents and voltages in transistor applications.

S. No.	Particular	Instantaneous a.c.	d.c.	Total
1.	Emitter current	i_e	I_E	i_E
2.	Collector current	i_c	I_C	i_C
3.	Base current	i_b	I_B	i_B
4.	Collector-emitter voltage	v_{ce}	V_{CE}	v_{CE}
5.	Emitter-base voltage	v_{eb}	V_{EB}	v_{EB}

8.17 Transistor Load Line Analysis

In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages. One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as *load line method* can be used to solve such problems. As explained later in this section, this method is quite easy and is frequently used in the analysis of transistor applications.

---

* If d.c. bias voltage is not provided, then during negative half-cycle of the signal, the emitter-base junction will be reverse biased. This will upset the transistor action.

** Throughout the book, we shall use sine wave signals because these are convenient for testing amplifiers. But it must be realised that signals (*e.g.* speech, music etc.) with which we work are generally complex having little resemblance to a sine wave. However, fourier series analysis tells us that such complex signals may be expressed as a sum of sine waves of various frequencies.

d.c. load line. Consider a common emitter *npn* transistor circuit shown in Fig. 8.35 (*i*) wh signal is applied. Therefore, d.c. conditions prevail in the circuit. The output characteristics circuit are shown in Fig. 8.35 (*ii*).

The value of collector-emitter voltage V_{CE} at any time is given by ;

$$V_{CE} = V_{CC} - I_C R_C$$

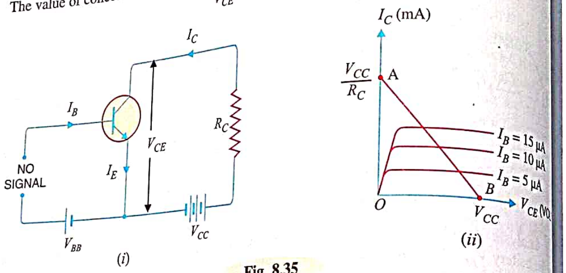


Fig. 8.35

As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represen a straight line on the output characteristics. This is known as *d.c. load line* and determines the of $V_{CE} - I_C$ points for any given value of R_C. To add load line, we need two end points of the st line. These two points can be located as under :

(*i*) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equ V_{CC} *i.e.*

$$\text{Max. } V_{CE} = V_{CC} - I_C R_C$$
$$= V_{CC} \qquad (\because I_C = 0)$$

This gives the first point B ($OB = V_{CC}$) on the collector-emitter voltage axis as show Fig. 8.35 (*ii*).

(*ii*) When collector-emitter voltage $V_{CE} = 0$, the collector current is maximum and is equ V_{CC}/R_C *i.e.*

$$V_{CE} = V_{CC} - I_C R_C$$

or

$$0 = V_{CC} - I_C R_C$$

$\therefore$

$$\text{Max. } I_C = V_{CC}/R_C$$

This gives the second point A ($OA = V_{CC}/R_C$) on the collector current axis as shown in Fig. 8.35 (*ii*). By joining these two points, d.c. *load line AB is constructed.

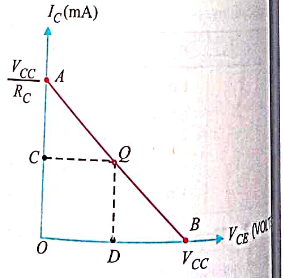


Fig. 8.36

Importance. The current (I_C) and voltage (V_{CE}) conditions in the transistor circuit are represented by some point on the output characteristics. The same information can be obtained from the load line. Thus when I_C is maximum (= V_{CC}/R_C), then $V_{CE} = 0$ as shown in Fig. 8.36. If $I_C = 0$, then V_{CE} is maximum and is equal to V_{CC}. For any other value of collector current say OC, the collector-emitter voltage $V_{CE} = OD$. It follows, therefore, that load line gives a far more convenient and direct solution to the problem.

Note. If we plot the load line on the output characteristic of the transistor, we can investigate the behaviour of the transistor amplifier. It is because we have the transistor output current and voltage specified in the form of load line equation and the transistor behaviour itself specified implicitly by the output characteristics.

8.18 Operating Point

The zero signal values of I_C and V_{CE} are known as the **operating point**.

It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also called quiescent (silent) point or *Q-point* because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent *i.e.* in the absence of the signal.

Suppose in the absence of signal, the base current is 5 μA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on $I_B = 5\ \mu A$ characteristic. But I_C and V_{CE} conditions in the circuit should also be represented by some point on the d.c. load line AB. The point Q where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point Q describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point. Referring to Fig. 8.37, for $I_B = 5\ \mu A$, the zero signal values are :

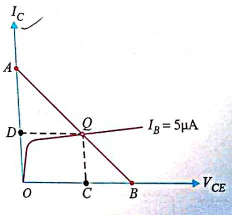


Fig. 8.37

$$V_{CE} = OC \text{ volts}$$
$$I_C = OD \text{ mA}$$

It follows, therefore, that the zero signal values of I_C and V_{CE} (*i.e.* operating point) are determined by the point where d.c. load line intersects the proper base current curve.

Example 8.22. *For the circuit shown in Fig. 8.38 (i), draw the d.c. load line.*

Solution. The collector-emitter voltage V_{CE} is given by ;

$$V_{CE} = V_{CC} - I_C R_C \qquad \text{...(i)}$$

When $I_C = 0$, then,

$$V_{CE} = V_{CC} = 12.5 \text{ V}$$

This locates the point B of the load line on the collector-emitter voltage axis.

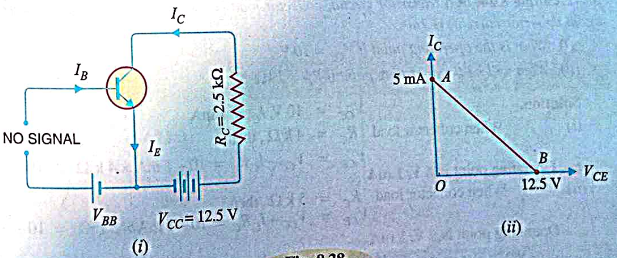
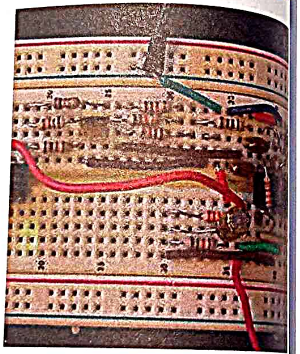


Fig. 8.38

Why load line ? The resistance R_C connected to the device is called load or load resistance for the ci and, therefore, the line we have just constructed is called the load line.

9

Transistor Biasing



INTRODUCTION

The basic function of transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*. In order to achieve this, means are provided to ensure that input circuit (*i.e.* base-emitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector-base junction) always remains reverse biased during all parts of the signal. This is known as transistor biasing. In this chapter, we shall discuss how transistor biasing helps in achieving faithful amplification.

9.1 Faithful Amplification

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

(*i*) **Proper zero signal collector current.** Consider an *npn* transistor circuit shown in Fig. 9.1 (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.

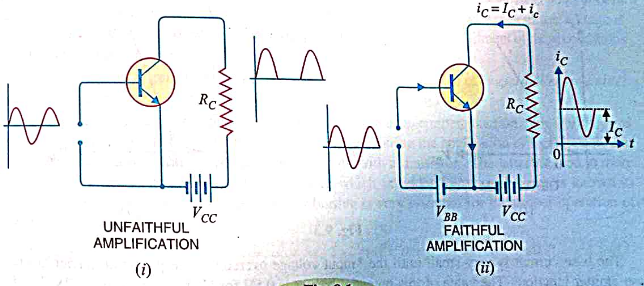


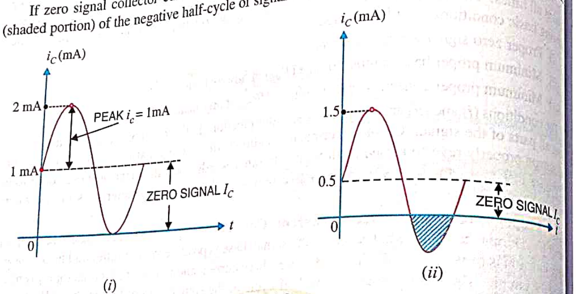
Fig. 9.1

Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. 9.1 (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as *zero signal collector current* I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. *The value of zero signal collector current should be atleast equal to the maximum collector current due to signal alone i.e.*

Zero signal collector current $\geq$ Max. collector current due to signal alone

Illustration. Suppose a signal applied to the base of a transistor gives a peak collector current 1mA. Then zero signal collector current must be atleast equal to 1mA so that even during the peak negative half-cycle of the signal, there is no cut off as shown in Fig. 9.2 (*i*).

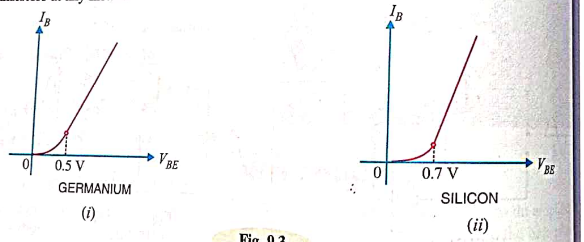
If zero signal collector current is less, say 0.5 mA as shown in Fig. 9.2 (*ii*), then some (shaded portion) of the negative half-cycle of signal will be cut off in the output.



(*i*) (*ii*)

Fig. 9.2

(*ii*) **Proper minimum base-emitter voltage.** In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for transistors at any instant.



(*i*) (*ii*)

Fig. 9.3

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for transistors as shown in Fig. 9.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

(*iii*) **Proper minimum V_{CE} at any instant.** For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called *knee voltage* (See Fig. 9.4).

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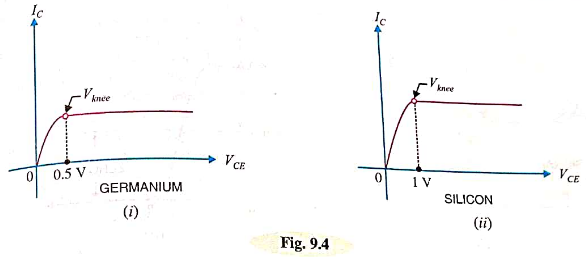
* In practice, a.c. signals have small voltage level (< 0.1V) and if applied directly will not give any collector current.



(*i*) (*ii*)

Fig. 9.4

When V_{CE} is too low (less than 0.5V for *Ge* transistors and 1V for *Si* transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

9.2 Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely : (*i*) proper zero signal collector current, (*ii*) proper base-emitter voltage at any instant and (*iii*) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

" *The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as* **transistor biasing.** "

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as *biasing circuit*. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Example 9.1. *An npn silicon transistor has V_{CC} = 6 V and the collector load R_C = 2.5 kΩ. Find :*

(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.

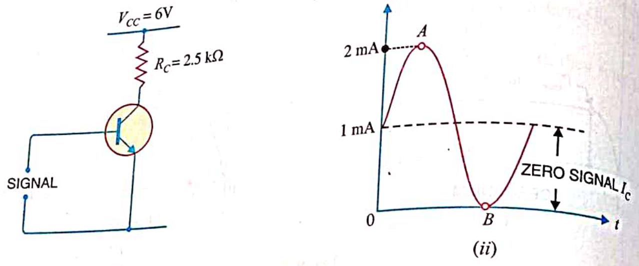
(ii) The minimum zero signal collector current required.

Solution.
Collector supply voltage, V_{CC} = 6 V
Collector load, R_C = 2.5 kΩ

(*i*) We know that for faithful amplification, V_{CE} should not be less than 1V for silicon transistor.

$\therefore$ Max. voltage allowed across R_C = 6 − 1 = 5 V

$\therefore$ Max. allowed collector current = 5 V/R_C = 5 V/2.5 kΩ = **2 mA**



(i) (ii)

Fig. 9.5

Thus, the maximum collector current allowed during any part of the signal is 2 mA. If the collector current is allowed to rise above this value, V_{CE} will fall below 1 V. Consequently, value of β will fall, resulting in unfaithful amplification.

(ii) During the negative peak of the signal, collector current can at the most be allowed to become zero. As the negative and positive half cycles of the signal are equal, therefore, the change in collector current due to these will also be equal but in opposite direction.

∴ Minimum zero signal collector current required = 2 mA/2 = **1 mA**

During the positive peak of the signal [point *A* in Fig. 9.5 *(ii)*], $i_C = 1 + 1 = 2$mA and during the negative peak (point *B*),

$$i_C = 1 - 1 = 0 \text{ mA}$$

Example 9.2. *A transistor employs a 4 kΩ load and $V_{CC} = 13V$. What is the maximum input signal if β = 100 ? Given $V_{knee} = 1V$ and a change of 1V in V_{BE} causes a change of 5mA in collector current.*

Solution.

Collector supply voltage, V_{CC} = 13 V

Knee voltage, V_{knee} = 1 V

Collector load, R_C = 4 kΩ

∴ Max. allowed voltage across R_C = 13 − 1 = 12 V

$$\therefore \text{ Max. allowed collector current, } i_C = \frac{12\text{ V}}{R_C} = \frac{12\text{ V}}{4\text{ k}\Omega} = 3\text{ mA}$$

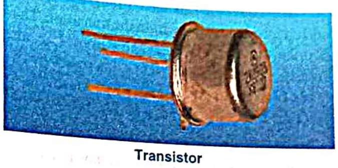
$$\text{Maximum base current, } i_B = \frac{i_C}{\beta} = \frac{3\text{ mA}}{100} = 30\ \mu\text{A}$$

$$\text{Now} \quad \frac{\text{Collector current}}{\text{Base voltage (signal voltage)}} = 5\text{ mA/V}$$

$$\therefore \quad \text{Base voltage (signal voltage)} = \frac{\text{Collector current}}{5\text{ mA/V}} = \frac{3\text{ mA}}{5\text{ mA/V}} = \mathbf{600\ mV}$$

9.3 Inherent Variations of Transistor Parameters

In practice, the transistor parameters such as β, V_{BE} are not the same for every transistor even of the same type. To give an example, BC147 is a silicon *npn* transistor with β varying from 100 to 600 *i.e.* β for one transistor may be 100 and for the other it may be 600, although both of them are *BC147*. This large variation in parameters is a characteristic of transistors. The major reason for these variations is that transistor is a new device and manufacturing techniques have not too much advanced. For instance, it has not been possible to control the base width and it may vary, although slightly, from one transistor to the other even of the same type. Such small variations result in large change in transistor parameters such as β, V_{BE} etc.



Transistor

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. It is, therefore, very important that biasing network be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. In other words, the operating point should be independent of transistor parameters variations.

9.4 Stabilisation

The collector current in a transistor changes rapidly when

(i) the temperature changes,

(ii) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons :

(i) Temperature dependence of I_C

(ii) Individual variations

(iii) Thermal runaway

(i) **Temperature dependence of I_C.** The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant inspite of temperature variations.

(ii) **Individual variations.** The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point *i.e.* to hold I_C constant irrespective of individual variations in transistor parameters.

(iii) **Thermal runaway.** The collector current for a *CE* configuration is given by : ...*(i)*

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collec current produces heat within the transistor. This raises the transistor temperature and if no stabilisatio is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (*i*) that if I_{CBO} creases, the collector current I_C increases by $(\beta + 1)\, I_{CBO}$. The increased I_C will raise the temperat of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter seconds, the collector current may become very large, causing the transistor to burn out. *The self-destruction of an unstabilised transistor is known as* **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essent that operating point is stabilised *i.e.* I_C is kept constant. In practice, this is done by causing I_B decrease automatically with temperature increase by circuit modification. Then decrease in βI_B wi compensate for the increase in $(\beta + 1)\, I_{CBO}$, keeping I_C nearly constant. In fact, this is what is alwa aimed at while building and designing a biasing circuit.

9.5 Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification. The biasing network associated with the transistor should meet the following requirements :

(*i*) It should ensure proper zero signal collector current.

(*ii*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silico transistors at any instant.

(*iii*) It should ensure the stabilisation of operating point.

9.6 Stability Factor

It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measure by stability factor *S*. It is defined as under :

*The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} at constant and I_B is called* **stability factor** *i.e.*

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \quad \text{at constant } I_B \text{ and } \beta$$

The stability factor indicates the change in collector current I_C due to the change in collecto leakage current I_{CO}. Thus a stability factor 50 of a circuit means that I_C changes 50 times as much a any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stabilit factor as possible. The ideal value of *S* is 1 but it is never possible to achieve it in practice. Exper ence shows that values of S exceeding 25 result in unsatisfactory performance.

The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1)\, I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

or

$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{CO}}{dI_C} = \frac{1}{S}\right]$$

or

$$S = \frac{\beta + 1}{1 - \beta\left(\dfrac{dI_B}{dI_C}\right)}$$

---

* $I_{CBO} = I_{CO}$ = collector leakage current in CB arrangement

** Assuming β to be independent of I_C

9.7 Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from the battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (*i.e.* V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e.* V_{CC}) :

(*i*) Base resistor method

(*ii*) Emitter bias method

(*iii*) Biasing with collector-feedback resistor

(*iv*) Voltage-divider bias

In all these methods, the same basic principle is employed *i.e.* required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is selected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1 V for silicon transistors.

For example, if $\beta = 100$ and the zero signal collector current I_C is to be set at 1mA, then I_B is made equal to $I_C/\beta = 1/100 = 10\ \mu A$. Thus, the biasing network should be so designed that a base current of 10 μA flows in the zero signal conditions.

9.8 Base Resistor Method

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig. 9.6) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

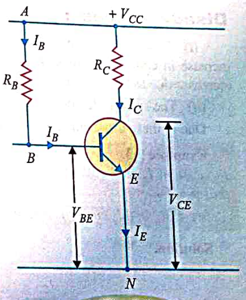


Fig. 9.6

Circuit analysis. It is required to find the value of R_B so that required collector current flows in the zero signal conditions. Let I_C be the required zero signal collector current.

$$\therefore \quad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or

$$I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad \text{... } (i)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (*i*).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from exp. (*i*) that :

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence R_B can always be found directly, and for this reason, this method is sometimes called ***fixed-bias method***.

Stability factor. As shown in Art. 9.6,

$$\text{Stability factor,} \quad S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$. Putting the value of $dI_B / dI_C = 0$ in the above expression, we have,

$$\text{Stability factor,} \quad S = \beta + 1$$

Thus the stability factor in a fixed bias is ($\beta + 1$). This means that I_C changes ($\beta + 1$) times as much as any change in I_{CO}. For instance, if $\beta = 100$, then $S = 101$ which means that I_C increases 101 times faster than I_{CO}. Due to the large value of S in a fixed bias, it has poor thermal stability.

Advantages :

(*i*) This biasing circuit is very simple as only one resistance R_B is required.

(*ii*) Biasing conditions can easily be set and the calculations are simple.

(*iii*) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages :

(*i*) This method provides poor stabilisation. It is because there is no means to stop a self-increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

(*ii*) The stability factor is very high. Therefore, there are strong chances of thermal runaway.

Due to these disadvantages, this method of biasing is rarely employed.

Example 9.3. *Fig. 9.7 (i) shows biasing with base resistor method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE}. Neglect small base-emitter voltage. Given that $\beta = 50$.*

(ii) If R_B in this circuit is changed to 50 kΩ, find the new operating point.

Solution.

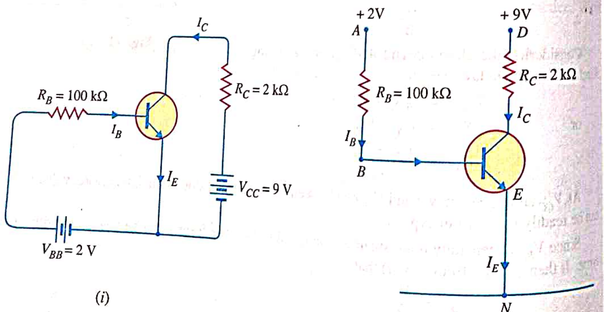


Fig. 9.7

In the circuit shown in Fig. 9.7 (*i*), biasing is provided by a battery V_{BB} (= 2V) in the base circuit which is separate from the battery V_{CC} (= 9V) used in the output circuit. The same circuit is shown in a simplified way in Fig. 9.7 (*ii*). Here, we need show only the supply voltages, + 2V and + 9V. It may be noted that negative terminals of the power supplies are grounded to get a complete path of current.

(*i*) Referring to Fig.9.7 (*ii*) and applying Kirchhoff's voltage law to the circuit *ABEN*, we get,

$$I_B R_B + V_{BE} = 2 \text{ V}$$

As V_{BE} is negligible,

$$\therefore \quad I_B = \frac{2\text{V}}{R_B} = \frac{2\text{V}}{100 \text{ k}\Omega} = 20 \ \mu\text{A}$$

$$\text{Collector current, } I_C = \beta I_B = 50 \times 20 \ \mu\text{A} = 1000 \ \mu\text{A} = \mathbf{1 \ mA}$$

Applying Kirchhoff's voltage law to the circuit *DEN*, we get,

$$I_C R_C + V_{CE} = 9$$

or

$$1 \text{ mA} \times 2 \text{ k}\Omega + V_{CE} = 9$$

or

$$V_{CE} = 9 - 2 = \mathbf{7 \ V}$$

(*ii*) When R_B is made equal to 50 kΩ, then it is easy to see that base current is doubled *i.e.* $I_B = 40 \ \mu$A.

$$\therefore \quad \text{Collector current, } I_C = \beta I_B = 50 \times 40 = 2000 \ \mu\text{A} = 2 \text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C R_C = 9 - 2 \text{ mA} \times 2 \text{ k}\Omega = 5 \text{ V}$$

∴ New operating point is **5 V, 2 mA.**

Example 9.4. *Fig. 9.8 (i) shows that a silicon transistor with $\beta = 100$ is biased by base resistor method. Draw the d.c. load line and determine the operating point. What is the stability factor ?*

Solution. $V_{CC} = 6$ V, $R_B = 530$ kΩ, $R_C = 2$ kΩ

D.C. load line. Referring to Fig. 9.8 (*i*), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V. This locates the first point B (OB = 6V) of the load line on collector-emitter voltage axis as shown in Fig. 9.8 (*ii*).

When $V_{CE} = 0$, $I_C = V_{CC}/R_C$ = 6V/2 kΩ = 3 mA. This locates the second point A (OA = 3mA) of the load line on the collector current axis. By joining points A and B, d.c. load line AB is constructed [See Fig. 9.8 (*ii*)].

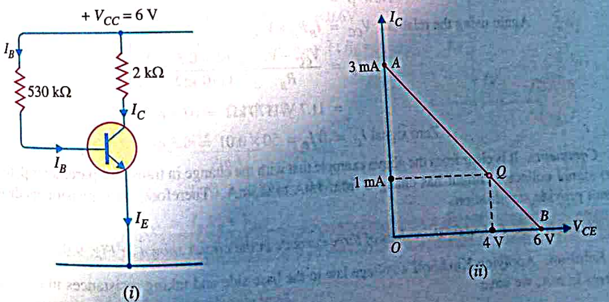


Fig. 9.8

Operating point Q. As it is a silicon transistor, therefore, $V_{BE} = 0.7V$. Referring to Fig. 9.8 (i), it is clear that :

$$I_B R_B + V_{BE} = V_{CC}$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6 - 0.7)\ \text{V}}{530\ \text{k}\Omega} = 10\ \mu\text{A}$$

Collector current, $I_C = \beta I_B = 100 \times 10 = 1000\ \mu\text{A} = 1\ \text{mA}$

$\therefore$ Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 6 - 1\ \text{mA} \times 2\ \text{k}\Omega = 6 - 2 = 4\ \text{V}$

$\therefore$ Operating point is **4 V, 1 mA.**

Fig. 9.8 (*ii*) shows the operating point Q on the d.c. load line. Its co-ordinates are $I_C = 1\text{mA}$ and $V_{CE} = 4\text{V}$.

$$\text{Stability factor} = \beta + 1 = 100 + 1 = \mathbf{101}$$

Example 9.5. *(i) A germanium transistor is to be operated at zero signal $I_C = 1mA$. If the collector supply $V_{CC} = 12V$, what is the value of R_B in the base resistor method ? Take $\beta = 100$.*

(ii) If another transistor of the same batch with $\beta = 50$ is used, what will be the new value of zero signal I_C for the same R_B ?

Solution. $V_{CC} = 12\ \text{V}, \quad \beta = 100$

As it is a *Ge* transistor, therefore,

$$V_{BE} = 0.3\ \text{V}$$

(*i*) Zero signal $I_C = 1\ \text{mA}$

$\therefore$ Zero signal $I_B = I_C/\beta = 1\ \text{mA}/100 = 0.01\ \text{mA}$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.3}{0.01\ \text{mA}}$$

$$= 11.7\ \text{V}/0.01\ \text{mA} = \mathbf{1170\ k\Omega}$$

(*ii*) Now $\beta = 50$

Again using the relation, $V_{CC} = I_B R_B + V_{BE}$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.3}{1170\ \text{k}\Omega}$$

$$= 11.7\ \text{V}/1170\ \text{k}\Omega = 0.01\ \text{mA}$$

$\therefore$ Zero signal $I_C = \beta I_B = 50 \times 0.01 = \mathbf{0.5\ mA}$

Comments. It is clear from the above example that with the change in transistor parameter β, the zero signal collector current has changed from 1mA to 0.5mA. Therefore, base resistor method cannot provide stabilisation.

Example 9.6. *Calculate the values of three currents in the circuit shown in Fig. 9.9.*

Solution. Applying Kirchhoff's voltage law to the base side and taking resistances in kΩ and currents in mA, we have,

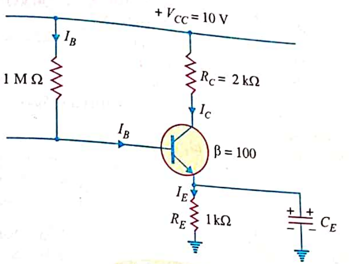


Fig. 9.9

$$V_{CC} = I_B R_B + V_{BE} + I_E \times 1$$

or $\quad 10 = 1000\, I_B + {}^*0 + (I_C + I_B)$

or $\quad 10 = 1000\, I_B + (\beta\, I_B + I_B)$

or $\quad 10 = 1000\, I_B + (100\, I_B + I_B)$

or $\quad 10 = 1101\, I_B$

$\therefore \quad I_B = 10/1101 = \mathbf{0.0091\ mA}$

$$I_C = \beta\, I_B = 100 \times 0.0091 = \mathbf{0.91\ mA}$$

$$I_E = I_C + I_B = 0.91 + 0.0091 = \mathbf{0.919\ mA}$$

Example 9.7. *Design base resistor bias circuit for a CE amplifier such that operating point is $V_{CE} = 8V$ and $I_C = 2$ mA. You are supplied with a fixed 15V d.c. supply and a silicon transistor with $\beta = 100$. Take base-emitter voltage $V_{BE} = 0.6V$. Calculate also the value of load resistance that would be employed.*

Solution. Fig. 9.10 shows *CE* amplifier using base resistor method of biasing.

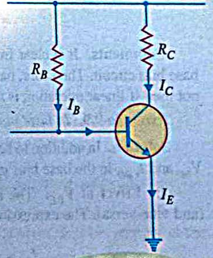


Fig. 9.10

$$V_{CC} = 15\ \text{V}\ ;\ \beta = 100\ ;\ V_{BE} = 0.6\text{V}$$

$$V_{CE} = 8\ \text{V}\ ;\ I_C = 2\ \text{mA};\ R_C = ?\ ;\ R_B = ?$$

$$V_{CC} = V_{CE} + I_C R_C$$

or $\quad 15\ \text{V} = 8\ \text{V} + 2\ \text{mA} \times R_C$

$$\therefore \quad R_C = \frac{(15 - 8)\ \text{V}}{2\text{mA}} = \mathbf{3.5\ k\Omega}$$

$$I_B = I_C/\beta = 2/100 = 0.02\ \text{mA}$$

$$V_{CC} = I_B R_B + V_{BE}$$

---

* Neglecting V_{BE} as it is generally very small.

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{(15 - 0.6)\text{ V}}{0.02\text{ mA}} = \mathbf{720\ k\Omega}$$

Example 9.8. *A *base bias circuit in Fig. 9.11 is subjected to an increase in temperature from 25°C to 75°C. If β = 100 at 25°C and 150 at 75°C, determine the percentage change in Q-point values (V_{CE} and I_C) over this temperature range. Neglect any change in V_{BE} and the effects of any leakage current.*

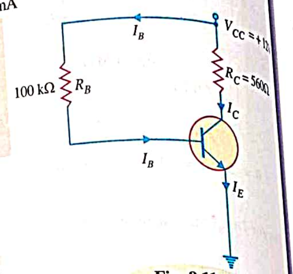


Fig. 9.11

Solution.

At 25°C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{100\ k\Omega} = 0.113\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 100 \times 0.113\text{ mA} = 11.3\text{ mA}$$

$$\text{and} \quad V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (11.3\text{ mA})\ (560\Omega) = 5.67\text{V}$$

At 75 °C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = 0.113\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 150 \times 0.113\text{ mA} = 17\text{ mA}$$

$$\text{and} \quad V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (17\text{ mA})\ (560\ \Omega) = 2.48\text{V}$$

$$\%\text{age change in } I_C = \frac{I_{C\,(75°C)} - I_{C\,(25°C)}}{I_{C\,(25°C)}} \times 100$$

$$= \frac{17\text{ mA} - 11.3\text{ mA}}{11.3\text{ mA}} \times 100 = \mathbf{50\%}\ \textit{(increase)}$$

Note that I_C changes by the same percentage as β.

$$\%\text{age change in } V_{CE} = \frac{V_{CE\,(75°C)} - V_{CE\,(25°C)}}{V_{CE\,(25°C)}} \times 100$$

$$= \frac{2.48\text{V} - 5.67\text{V}}{5.67\text{V}} \times 100 = -\mathbf{56.3\%}\ \textit{(decrease)}$$

Comments. It is clear from the above example that Q-point is extremely dependent on β in a base bias circuit. Therefore, base bias circuit is very unstable. Consequently, this method is normally not used if linear operation is required. However, it can be used for switching operation.

Example 9.9. *In base bias method, how Q-point is affected by changes in V_{BE} and I_{CBO}.*

Solution. In addition to being affected by change in β, the Q-point is also affected by changes in V_{BE} and I_{CBO} in the base bias method.

(*i*) **Effect of V_{BE}.** The base-emitter-voltage V_{BE} decreases with the increase in temperature (and vice-versa). The expression for I_B in base bias method is given by ;

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

---

* Note that base resistor method is also called *base bias method*.

It is clear that decrease in V_{BE} increases I_B. This will shift the Q-point ($I_C = \beta I_B$ and $V_{CE} = V_{CC} - I_C R_C$). The effect of change in V_{BE} is negligible if $V_{CC} >> V_{BE}$ (V_{CC} atleast 10 times greater than V_{BE}).

(*ii*) **Effect of I_{CBO}.** The reverse leakage current I_{CBO} has the effect of decreasing the net base current and thus increasing the base voltage. It is because the flow of I_{CBO} creates a voltage drop across R_B that adds to the base voltage as shown in Fig. 9.12. Therefore, change in I_{CBO} shifts the Q-point of the base bias circuit. However, in modern transistors, I_{CBO} is usually less than 100 nA and its effect on the bias is negligible if $V_{BB} >> I_{CBO} R_B$.

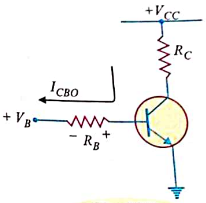
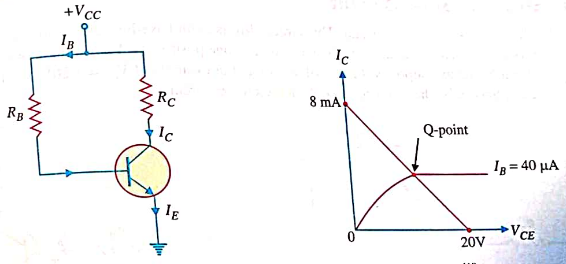


Fig. 9.12

Example 9.10. *Fig. 9.13 (i) shows the base resistor transistor circuit. The device (i.e. transistor) has the characteristics shown in Fig. 9.13 (ii). Determine V_{CC}, R_C and R_B.*



(*i*) (*ii*)

Fig. 9.13

Solution. From the d.c load line, V_{CC} = **20V.**

$$\text{Max. } I_C = \frac{V_{CC}}{R_C} \quad (\text{when } V_{CE} = 0\text{V})$$

$$\therefore \quad R_C = \frac{V_{CC}}{\text{Max. } I_C} = \frac{20\text{V}}{8\text{mA}} = \mathbf{2.5\ k\Omega}$$

$$\text{Now} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

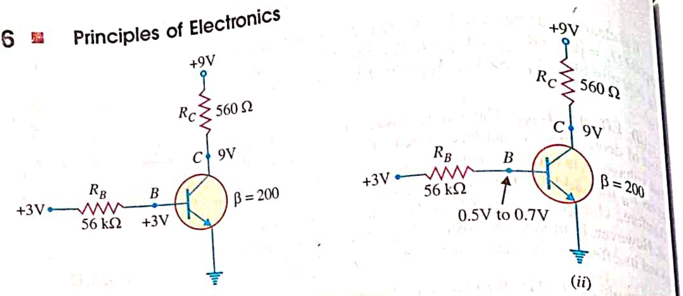
$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{V} - 0.7\text{V}}{40\ \mu\text{A}} = \frac{19.3\text{V}}{40\ \mu\text{A}} = \mathbf{482.5\ k\Omega}$$

Example 9.11. *What fault is indicated in (i) Fig. 9.14 (i) and (ii) Fig. 9.14 (ii) ?*

Solution.

(*i*) The obvious fault in Fig. 9.14 (*i*) is that the **base is internally open.** It is because 3V at the base and 9V at the collector mean that transistor is in cut-off state.

(*ii*) The obvious fault in Fig. 9.14 (*ii*) is that **collector is internally open.** The voltage at the base is correct. The voltage of 9V appears at the collector because the 'open' prevents collector current.



(i)

(ii)

Fig. 9.14

9.9 Emitter Bias Circuit

Fig. 9.15 shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources ; one positive (+ V_{CC}) and the other negative (– V_{EE}). Normally, the two supply voltages will be equal. For example, if V_{CC} = + 20V (d.c.), then V_{EE} = – 20V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.

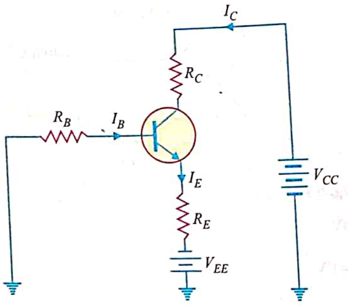


Fig. 9.15

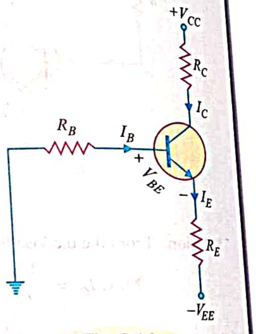


Fig. 9.16

We shall first redraw the circuit in Fig. 9.15 as it usually appears on schematic diagrams. This means deleting the battery symbols as shown in Fig. 9.16. All the information is still (See Fig. 9.16) on the diagram except that it is in condensed form. That is a negative supply voltage – V_{EE} is applied to the bottom of R_E and a positive voltage of + V_{CC} to the top of R_C.

9.10 Circuit Analysis of Emitter Bias

Fig. 9.16 shows the emitter bias circuit. We shall find the Q-point values (*i.e.* d.c. I_C and d.c. V_{CE}) for this circuit.

(*i*) **Collector current (I_C).** Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 9.16, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\therefore \quad V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore I_B \simeq \frac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$V_{EE} - V_{BE} = I_E (R_B/\beta + R_E)$$

$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

(*ii*) **Collector-emitter voltage (V_{CE}).** Fig. 9.17 shows the various voltages of the emitter bias circuit w.r.t. ground.

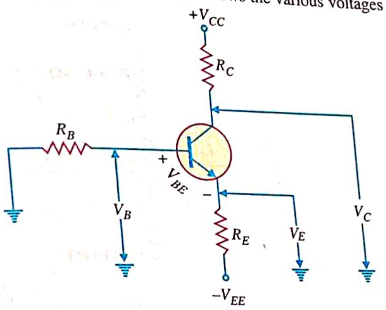


Fig. 9.17

Emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E$$

Base voltage w.r.t. ground is

$$V_B = V_E + V_{BE}$$

Collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C$$

Subtracting V_E from V_C and using the approximation $I_C \simeq I_E$, we have,

$$V_C - V_E = (V_{CC} - I_C R_C) - (-V_{EE} + I_C R_E) \qquad (\because I_E \simeq I_C)$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Alternatively. Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. 9.16 (Refer back), we have,

$$V_{CC} - I_C R_C - V_{CE} - I_C^{*} R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Stability of Emitter bias. The expression for collector current I_C for the emitter bias circuit is given by ;

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

---

* $I_C \approx I_E$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes :

$$I_C = \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes :

$$I_C (\simeq I_E) = \frac{V_{EE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of V_{BE}.

If $I_C (\simeq I_E)$ is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

Example 9.12. *For the emitter bias circuit shown in Fig. 9.18, find I_E, I_C, V_C and V_{CE} for $\beta = 85$ and $V_{BE} = 0.7V$.*

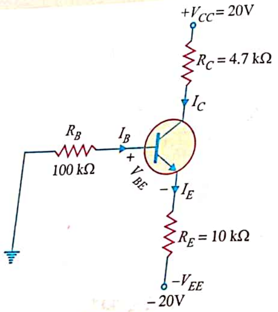


Fig. 9.18

Solution.

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.7V}{10 \text{ k}\Omega + 100 \text{ k}\Omega/85} = \mathbf{1.73 \text{ mA}}$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.73 \text{ mA})(4.7 \text{ k}\Omega) = \mathbf{11.9V}$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.73 \text{ mA})(10 \text{ k}\Omega) = -2.7V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.9 - (-2.7V) = \mathbf{14.6V}$$

Note that operating point (or Q – point) of the circuit is 14.6V, 1.73 mA.

Example 9.13. *Determine how much the Q-point in Fig. 9.18 (above) will change over a temperature range where β increases from 85 to 100 and V_{BE} decreases from 0.7V to 0.6V.*

Solution.

For $\beta = 85$ and $V_{BE} = 0.7V$

As calculated in the above example, $I_C = 1.73$ mA and $V_{CE} = 14.6V$.

For $\beta = 100$ and $V_{BE} = 0.6V$

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.6V}{10 \text{ k}\Omega + 100 \text{ k}\Omega/100} = \frac{19.4V}{11 \text{ k}\Omega} = 1.76 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.76 \text{ mA})(4.7 \text{ k}\Omega) = 11.7V$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.76 \text{ mA})(10 \text{ k}\Omega) = -2.4V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.7 - (-2.4) = 14.1V$$

$$\% \text{ age change in } I_C = \frac{1.76 \text{ mA} - 1.73 \text{ mA}}{1.73 \text{ mA}} \times 100 = \mathbf{1.7\%} \text{ (increase)}$$

$$\% \text{ age change in } V_{CE} = \frac{14.1V - 14.6V}{14.1V} \times 100 = \mathbf{-3.5\%} \text{ (decrease)}$$

9.11 Biasing with Collector Feedback Resistor

In this method, one end of R_B is connected to the base and the other end to the collector as shown in Fig. 9.19. Here, the required zero signal base current is determined *not* by V_{CC} but by the collector-base voltage V_{CB}. It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

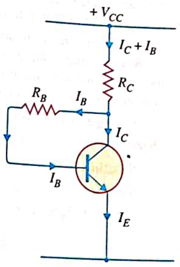


Fig. 9.19

Circuit analysis. The required value of R_B needed to give the zero signal current I_C can be determined as follows. Referring to Fig. 9.19,

$$V_{CC} = {}^{*}I_C R_C + I_B R_B + V_{BE}$$

or

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B} \quad (\because I_C = \beta I_B)$$

Alternatively, $V_{CE} = V_{BE} + V_{CB}$

or $V_{CB} = V_{CE} - V_{BE}$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}; \quad \text{where } I_B = \frac{I_C}{\beta}$$

It can be shown mathematically that stability factor S for this method of biasing is less than $(\beta + 1)$ *i.e.*

$$\text{Stability factor, } S < (\beta + 1)$$

Therefore, this method provides better thermal stability than the fixed bias.

Note. It can be easily proved (See **example 9.17) that Q-point values (I_C and V_{CE}) for the circuit shown in Fig. 9.19 are given by ;

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}$$

and

$$V_{CE} = V_{CC} - I_C R_C$$

Advantages

(*i*) It is a simple method as it requires only one resistance R_B.

(*ii*) This circuit provides some stabilisation of the operating point as discussed below :

$$V_{CE} = V_{BE} + V_{CB}$$

---

[*] Actually voltage drop across $R_C = (I_B + I_C) R_C$. However, $I_B << I_C$. Therefore, as a reasonable approximation, we can say that drop across $R_C = I_C R_C$.

[**] Put $R_E = 0$ for the expression of I_C in exmaple 9.17. It is because in the present circuit (Fig. 9.19), there is no R_E.

Suppose the temperature increases. This will increase collector leakage current and hence the total collector current. But as soon as collector current increases, V_{CE} decreases due to greater drop across R_C. The result is that V_{CB} decreases *i.e.* lesser voltage is available across R_B. Hence the base current I_B decreases. The smaller I_B tends to decrease the collector current to original value.

Disadvantages

(*i*) The circuit does not provide good stabilisation because stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and other effects.

(*ii*) This circuit provides a negative feedback which reduces the gain of the amplifier as explained hereafter. During the positive half-cycle of the signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current.

Example 9.14. *Fig. 9.20 shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that β = 100.*

Solution. $V_{CC} = 20\text{V}, R_B = 100\text{ k}\Omega, R_C = 1\text{k}\Omega$

Since it is a silicon transistor, $V_{BE} = 0.7\text{ V}$.

Assuming I_B to be in mA and using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B}$$

or $$100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1$$

or $$200\, I_B = 19.3$$

or $$I_B = \frac{19.3}{200} = 0.096\text{ mA}$$

∴ Collector current, $I_C = \beta\, I_B = 100 \times 0.096 = 9.6\text{ mA}$

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 20 - 9.6\text{ mA} \times 1\text{ k}\Omega$$
$$= 10.4\text{ V}$$

∴ Operating point is **10.4 V, 9.6 mA.**

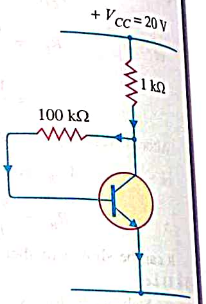


Fig. 9.20

Alternatively

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{20\text{V} - 0.7\text{V}}{100\text{ k}\Omega/100 + 1\text{ k}\Omega} = \frac{19.3\text{V}}{2\text{ k}\Omega} = \mathbf{9.65\text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{V} - 9.65\text{ mA} \times 1\text{ k}\Omega = \mathbf{10.35V}$$

A very slight difference in the values is due to manipulation of calculations.

Example 9.15. *(i) It is required to set the operating point by biasing with collector feedback resistor at $I_C = 1\text{mA}$, $V_{CE} = 8\text{V}$. If β = 100, $V_{CC} = 12\text{V}$, $V_{BE} = 0.3\text{V}$, how will you do it ?*

(ii) What will be the new operating point if β = 50, all other circuit values remaining the same ?

Solution. $V_{CC} = 12\text{V}, V_{CE} = 8\text{V}, I_C = 1\text{mA}$

$$\beta = 100, V_{BE} = 0.3\text{V}$$

(*i*) To obtain the required operating point, we should find the value of R_B.

Now, collector load is

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{(12 - 8)\text{ V}}{1\text{ mA}} = 4\text{ k}\Omega$$

Also $$I_B = \frac{I_C}{\beta} = \frac{1\text{ mA}}{100} = 0.01\text{ mA}$$

Using the relation, $$R_B = \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

$$= \frac{12 - 0.3 - 100 \times 0.01 \times 4}{0.01} = \mathbf{770\text{ k}\Omega}$$

(*ii*) Now β = 50, and other circuit values remain the same.

∴ $$V_{CC} = V_{BE} + I_B R_B + \beta\, I_B R_C$$

or $$12 = 0.3 + I_B (R_B + \beta\, R_C)$$

or $$11.7 = I_B (770 + 50 \times 4)$$

or $$I_B = \frac{11.7\text{ V}}{970\text{ k}\Omega} = 0.012\text{ mA}$$

∴ Collector current, $I_C = \beta\, I_B = 50 \times 0.012 = 0.6\text{ mA}$

∴ Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 12 - 0.6\text{ mA} \times 4\text{ k}\Omega = 9.6\text{ V}$

∴ New operating point is **9.6 V, 0.6 mA.**

Comments. It may be seen that operating point is changed when a new transistor with lesser β is used. Therefore, biasing with collector feedback resistor does not provide very good stabilisation. It may be noted, however, that change in operating point is less than that of base resistor method.

Example 9.16. *It is desired to set the operating point at 2V, 1mA by biasing a silicon transistor with collector feedback resistor R_B. If β = 100, find the value of R_B.*

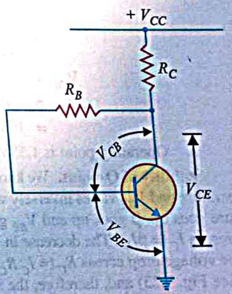


Fig. 9.21

Solution.

For a silicon transistor,

$$V_{BE} = 0.7\text{ V}$$

$$I_B = \frac{I_C}{\beta} = 1/100 = 0.01\text{ mA}$$

Now $$V_{CE} = V_{BE} + V_{CB}$$

or $$2 = 0.7 + V_{CB}$$

∴ $$V_{CB} = 2 - 0.7 = 1.3\text{ V}$$

∴ $$R_B = \frac{V_{CB}}{I_B} = \frac{1.3\text{V}}{0.01\text{ mA}} = \mathbf{130\text{ k}\Omega}$$

Example 9.17. *Find the Q-point values (I_C and V_{CE}) for the collector feedback bias circuit shown in Fig. 9.22.*

Solution. Fig. 9.22 shows the currents in the three resistors (R_C, R_B and R_E) in the circuit. By following the path through V_{CC}, R_C, R_B, V_{BE} and R_E and applying Kirchhoff's voltage law, we have,

$$V_{CC} - (I_C + I_B)\, R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Now $I_B + I_C \simeq I_C ; I_E \simeq I_C$ and $I_B = \frac{I_C}{\beta}$

$$\therefore \quad V_{CC} - I_C R_C - \frac{I_C}{\beta} R_B - V_{BE} - I_C R_E = 0$$

$$\text{or} \quad I_C \left(R_E + \frac{R_B}{\beta} + R_C\right) = V_{CC} - V_{BE}$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

Putting the given circuit values, we have,

$$I_C = \frac{12\text{V} - 0.7\text{V}}{1\text{ k}\Omega + 400\text{ k}\Omega/100 + 4\text{ k}\Omega}$$

$$= \frac{11.3\text{V}}{9\text{ k}\Omega} = 1.26\text{ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 12\text{V} - 1.26\text{ mA}\,(4\text{k}\Omega + 1\text{ k}\Omega)$$
$$= 12\text{V} - 6.3\text{V} = 5.7\text{V}$$

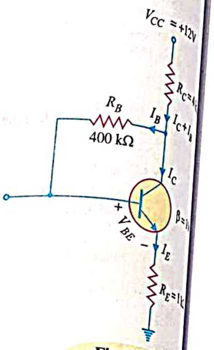


Fig. 9.22

∴ The operating point is **5.7V, 1.26 mA.**

Example 9.18. *Find the d.c. bias values for the collector-feedback biasing circuit shown in Fig. 9.23. How does the circuit maintain a stable Q point against temperature variations ?*

Solution. The collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

$$= \frac{10\text{V} - 0.7\text{V}}{0 + 100\text{ k}\Omega/100 + 10\text{ k}\Omega}$$

$$= \frac{9.3\text{V}}{11\text{ k}\Omega} = 0.845\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 10\text{V} - 0.845\text{ mA} \times 10\text{ k}\Omega$$
$$= 10\text{V} - 8.45\text{ V} = 1.55\text{V}$$

∴ Operating point is **1.55V, 0.845 mA.**

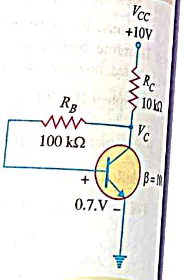


Fig. 9.23

Stability of Q-point. We know that β varies directly with temperature and V_{BE} varies inversely with temperature. As the temperature goes up, β goes up and V_{BE} goes down. The increase in β increases I_C ($= \beta I_B$). The decrease in V_{BE} increases I_B which in turn increases I_C. As I_C tries to increase the voltage drop across R_C ($= I_C R_C$) also tries to increases. This tends to reduce collector voltage V_C (See Fig. 9.23) and, therefore, the voltage across R_B. The reduced voltage across R_B reduces I_B and offsets the attempted increase in I_C and attempted decrease in V_C. The result is that the collector-feedback circuit maintains a stable Q-point. The reverse action occurs when the temperature decreases.

9.12 Voltage Divider Bias Method

This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} (See Fig. 9.24) and provide biasing. The emitter resistance R_E provides stabilisation. The name "voltage divider" comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero signal conditions.

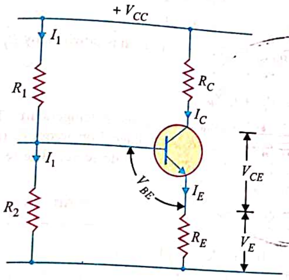


Fig. 9.24

Circuit analysis. Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

(*i*) **Collector current I_C :**

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

∴ Voltage across resistance R_2 is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit of Fig. 9.24,

$$V_2 = V_{BE} + V_E$$

$$\text{or} \quad V_2 = V_{BE} + I_E R_E$$

$$\text{or} \quad I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$\text{Since} \quad I_E \simeq I_C$$

$$\therefore \quad I_C = \frac{V_2 - V_{BE}}{R_E} \qquad \text{...(}i\text{)}$$

It is clear from exp. (*i*) above that I_C does not at all depend upon β. Though I_C depends upon V_{BE} but in practice $V_2 >> V_{BE}$ so that I_C is practically independent of V_{BE}. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured. It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

(*ii*) **Collector-emitter voltage V_{CE}.** Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilisation. In this circuit, excellent stabilisation is provided by R_E. Consideration of eq. (i) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across emitter resistance R_E to increase. As voltage drop across R_2 (*i.e.* V_2) is *independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor. It can be shown mathematically (See Art. 9.13) that stability factor of the circuit is given by :

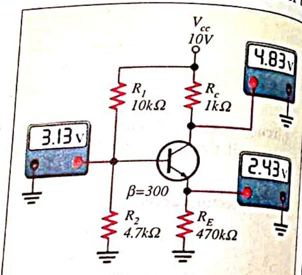
$$\text{Stability factor, } S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \dfrac{R_0}{R_E}}{\beta + 1 + \dfrac{R_0}{R_E}}$$

$$\text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 and the stability factor becomes :

$$\text{Stability factor} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$



A voltage divider biased transistor with correct voltages

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, R_0 / R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Example 9.19. *Fig. 9.25 (i) shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor to be of silicon.*

Solution.

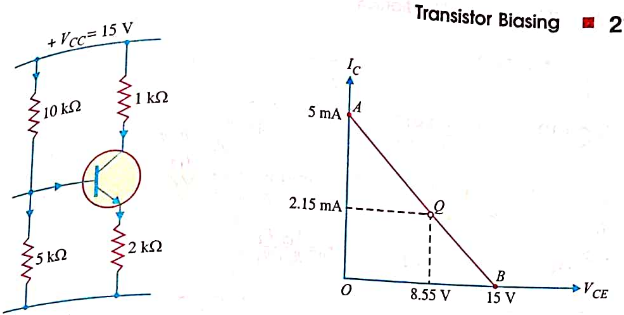
d.c. load line. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15$V. This locates the first point *B* (*OB* = 15V) of the load line on the collector-emitter voltage axis.

$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15 \text{ V}}{(1 + 2) \text{ k}\Omega} = 5 \text{ mA}$$

This locates the second point *A* (*OA* = 5 mA) of the load line on the collector current axis. By joining points *A* and *B*, the d.c. load line *AB* is constructed as shown in Fig. 9.25 (*ii*).



(*i*) (*ii*)

Fig. 9.25

Operating point. For silicon transistor,

$$V_{BE} = 0.7 \text{ V}$$

Voltage across 5 kΩ is

$$V_2 = \frac{V_{CC}}{10 + 5} \times 5 = \frac{15 \times 5}{10 + 5} = 5 \text{ V}$$

$$\therefore \quad \text{Emitter current, } I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2 \text{ k}\Omega} = \frac{4.3 \text{ V}}{2 \text{ k}\Omega} = 2.15 \text{ mA}$$

∴ Collector current is

$$I_C \simeq I_E = 2.15 \text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 15 - 2.15 \text{ mA} \times 3 \text{ k}\Omega = 15 - 6.45 = 8.55 \text{ V}$$

∴ Operating point is **8.55 V, 2.15 mA.**

Fig.9.25 (*ii*) shows the operating point *Q* on the load line. Its co-ordinates are $I_C = 2.15$ mA, $V_{CE} = 8.55$ V.

Example 9.20. *Determine the operating point of the circuit shown in the previous problem by using Thevenin's theorem.*

Solution. The circuit is redrawn and shown in Fig. 9.26 (*i*) for facility of reference. The d.c. circuit to the left of base terminal *B* can be replaced by Thevenin's equivalent circuit shown in Fig. 9.26 (*ii*). Looking to the left from the base terminal *B* [See Fig. 9.26 (*i*)], Thevenin's equivalent voltage E_0 is given by :

$$E_0 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{15}{10 + 5}\right) \times 5 = 5 \text{ V}$$

Again looking to the left from the base terminal *B* [See Fig. 9.26 (*i*)], Thevenin's equivalent resistance R_0 is given by :

$$R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

Fig. 9.26 (*ii*) shows the replacement of bias portion of the circuit of Fig. 9.26 (*i*) by its Thevenin's equivalent.

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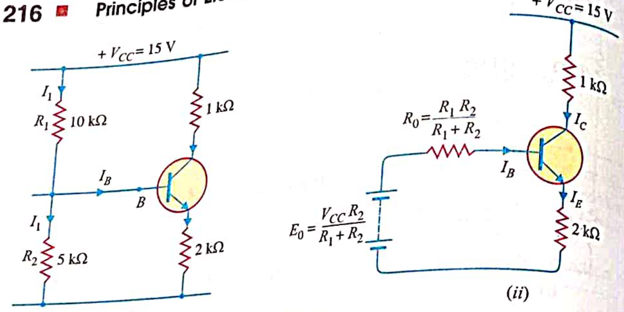
* Voltage drop across $R_2 = \left(\dfrac{V_{CC}}{R_1 + R_2}\right) R_2$

** Low value of R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restrictions on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same value of zero signal collector current. Therefore, the ratio R_0/R_E cannot be made very small from design point of view.



(i) (ii)

Fig. 9.26

Referring to Fig. 9.26 (ii), we have,

$$E_0 = I_B R_0 + V_{BE} + I_E R_E = I_B R_0 + V_{BE} + I_C R_E \qquad (\because I_E \simeq I_C)$$
$$= I_B R_0 + V_{BE} + \beta I_B R_E = I_B (R_0 + \beta R_E) + V_{BE}$$

or
$$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E}$$

$\therefore$ Collector current, $I_C = \beta I_B = \frac{\beta(E_0 - V_{BE})}{R_0 + \beta R_E}$

Dividing the numerator and denominator of R.H.S. by β, we get,

$$I_C = \frac{E_0 - V_{BE}}{\frac{R_0}{\beta} + R_E}$$

As *$R_0/\beta << R_E$, therefore, R_0/β may be neglected as compared to R_E.

$$\therefore \quad I_C = \frac{E_0 - V_{BE}}{R_E} = \frac{5 - 0.7}{2\ \text{k}\Omega} = 2.15\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 15 - 2.15\ \text{mA} \times 3\ \text{k}\Omega$$
$$= 15 - 6.45 = 8.55\ \text{V}$$

$\therefore$ Operating point is **8.55 V, 2.15 mA.**

Example 9.21. *A transistor uses potential divider method of biasing. $R_1 = 50\ k\Omega$, $R_2 = 10\ k\Omega$ and $R_E = 1 k\Omega$. If $V_{CC} = 12$ V, find :*

(i) the value of I_C ; given $V_{BE} = 0.1V$

(ii) the value of I_C ; given $V_{BE} = 0.3V$. Comment on the result.

Solution.
$$R_1 = 50\ \text{k}\Omega,\ R_2 = 10\ \text{k}\Omega,\ R_E = 1\ \text{k}\Omega,\ V_{CC} = 12\ \text{V}$$

(i) When $V_{BE} = 0.1$ V,

Voltage across R_2, $V_2 = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10}{50 + 10} \times 12 = 2$ V

$\therefore$ Collector current, $I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{2 - 0.1}{1\ \text{k}\Omega} = $ **1.9 mA**

---

* In fact, this condition means that I_B is very small as compared to I_1, the current flowing through R_1 and R_2.

(ii) When $V_{BE} = 0.3$ V,

Collector current, $I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{2 - 0.3}{1\ \text{k}\Omega} = $ **1.7 mA**

Comments. From the above example, it is clear that although V_{BE} varies by 300%, the value of I_C changes only by nearly 10%. This explains that in this method, I_C is almost independent of transistor parameter variations.

Example 9.22. *Calculate the emitter current in the voltage divider circuit shown in Fig. 9.27. Also find the value of V_{CE} and collector potential V_C.*

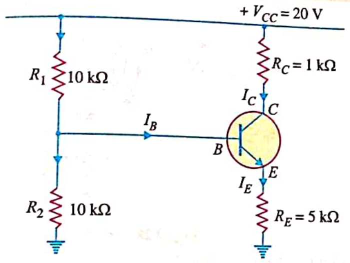


Fig. 9.27

Solution.

Voltage across R_2, $V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{20}{10 + 10}\right) 10 = 10$ V

Now $V_2 = V_{BE} + I_E R_E$

As V_{BE} is generally small, therefore, it can be neglected.

$$\therefore \quad I_E = \frac{V_2}{R_E} = \frac{10\ \text{V}}{5\ \text{k}\Omega} = \textbf{2 mA}$$

Now $I_C \simeq I_E = 2$ mA

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 2\ \text{mA}\ (6\ \text{k}\Omega)$$
$$= 20 - 12 = \textbf{8 V}$$

Collector potential, $V_C = V_{CC} - I_C R_C = 20 - 2\ \text{mA} \times 1\ \text{k}\Omega$
$$= 20 - 2 = \textbf{18 V}$$

9.13 Stability Factor For Potential Divider Bias

We have already seen (See example 9.20) how to replace the potential divider circuit of potential divider bias by Thevenin's equivalent circuit. The resulting potential divider bias circuit is redrawn in Fig. 9.28 in order to find the stability factor *S* for this biasing circuit. Referring to Fig. 9.28 and applying Kirchhoff's voltage law to the base circuit, we have,

$$E_0 - I_B R_0 - V_{BE} - I_E R_E = 0$$

or
$$E_0 = I_B R_0 + V_{BE} + (I_B + I_C) R_E$$

Considering V_{BE} to be constant and differentiating the above equation w.r.t. I_C, we have,

$$0 = R_0 \frac{dI_B}{dI_C} + 0 + R_E \frac{dI_B}{dI_C} + R_E$$

or $$0 = \frac{dI_B}{dI_C}(R_0 + R_E) + R_E$$

∴ $$\frac{dI_B}{dI_C} = \frac{-R_E}{R_0 + R_E} \qquad ...(i)$$

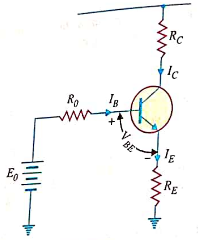


Fig. 9.28

The general expression for stability factor is

$$\text{Stability factor, } S = \frac{\beta + 1}{1 - \beta \dfrac{dI_B}{dI_C}}$$

Putting the value of dI_B/dI_C from eq. (*i*) into the expression for S, we have,

$$S = \frac{\beta + 1}{1 - \beta \dfrac{-R_E}{R_0 + R_E}} = \frac{\beta + 1}{1 + \left(\dfrac{\beta R_E}{R_0 + R_E}\right)}$$

$$= \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E} = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E(\beta + 1)}$$

∴ $$S = (\beta + 1) \times \frac{R_0 + R_E}{R_E(\beta + 1) + R_0}$$

Dividing the numerator and denominator of R.H.S. of the above equation by R_E, we have,

$$S = (\beta + 1) \times \frac{1 + R_0/R_E}{\beta + 1 + R_0/R_E} \qquad ...(ii)$$

Eq. (*ii*) gives the formula for the stability factor S for the potential divider bias circuit. The following points may be noted carefully :

(*i*) For greater thermal stability, the value of S should be small. This can be achieved by making R_0/R_E small. If R_0/R_E is made very small, then it can be neglected as compared to 1.

∴ $$S = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$

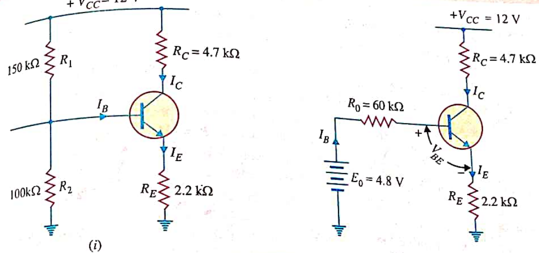
This is the ideal value of S and leads to the maximum thermal stability.

(*ii*) The ratio *R_0/R_E can be made very small by decreasing R_0 and increasing R_E. Low value of R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restriction on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same zero signal collector current. Due to these limitations, a compromise is made in the selection of the values of R_0 and R_E. Generally, these values are so selected that $S \simeq 10$.

---

* Remember, R_0 = Thevenin's equivalent resistance = $\dfrac{R_1 R_2}{R_1 + R_2}$

Example 9.23. *For the circuit shown in Fig. 9.29 (i), find the operating point. What is the stability factor of the circuit ? Given that $\beta = 50$ and $V_{BE} = 0.7V$.*



(*i*) (*ii*)

Fig. 9.29

Solution. Fig. 9.29 (*i*) shows the circuit of potential divider bias whereas Fig. 9.29 (*ii*) shows it with potential divider circuit replaced by Thevenin's equivalent circuit.

$$E_0 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{12V}{150\text{ k}\Omega + 100\text{ k}\Omega} \times 100\text{ k}\Omega = 4.8V$$

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{150\text{ k}\Omega \times 100\text{ k}\Omega}{150\text{ k}\Omega + 100\text{ k}\Omega} = 60\text{ k}\Omega$$

∴ $$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E} \qquad \text{...... (See Ex. 9.20)}$$

$$= \frac{4.8V - 0.7V}{60\text{ k}\Omega + 50 \times 2.2\text{ k}\Omega} = \frac{4.1V}{170\text{ k}\Omega} = 0.024\text{ mA}$$

Now $$I_C = \beta I_B = 50 \times 0.024 = 1.2\text{ mA}$$

∴ $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 12V - 1.2mA\,(4.7\text{ k}\Omega + 2.2\text{ k}\Omega) = 3.72V$$

∴ Operating point is **3.72V, 1.2 mA.**

Now $$\frac{R_0}{R_E} = \frac{60\text{ k}\Omega}{2.2\text{ k}\Omega} = 27.3$$

∴ Stability factor, $$S = (\beta + 1) \times \frac{1 + R_0/R_E}{\beta + 1 + R_0/R_E}$$

$$= (50 + 1) \times \frac{1 + 27.3}{50 + 1 + 27.3} = \mathbf{18.4}$$

Note. We can also find the value of I_C and V_{CE} (See Art. 9.12) as under :

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{where } V_2 = \frac{V_{CC}}{R_1 + R_2} \times R_2$$

and $$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

However, by replacing the potential divider circuit by Thevenin's equivalent circuit, the expression for I_C can be found more accurately. If not mentioned in the problem, any one of the two methods can be used to obtain the solution.

Example 9.24. *The circuit shown in Fig. 9.30 (i) uses silicon transistor having β = 100. Find the operating point and stability factor.*

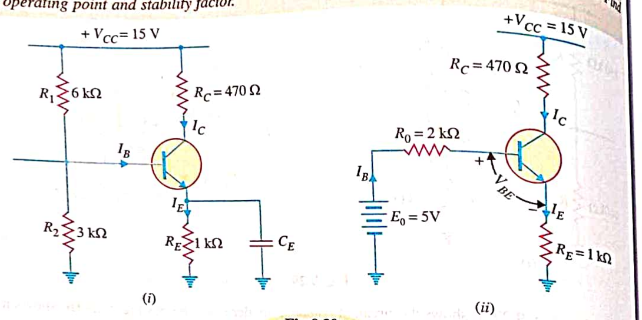


Fig 9.30

Solution. Fig. 9.30 (*i*) shows the circuit of potential divider bias whereas Fig. 9.30 (*ii*) shows it with potential divider circuit replaced by Thevenin's equivalent circuit.

$$E_0 = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{15\text{V}}{6\text{ k}\Omega + 3\text{ k}\Omega} \times 3\text{ k}\Omega = \frac{15\text{V}}{9\text{ k}\Omega} \times 3\text{ k}\Omega = 5\text{V}$$

$$R_0 = \frac{R_1 R_2}{R_1 + R_2} = \frac{6\text{ k}\Omega \times 3\text{ k}\Omega}{6\text{ k}\Omega + 3\text{ k}\Omega} = 2\text{ k}\Omega$$

Now $$I_B = \frac{E_0 - V_{BE}}{R_0 + \beta R_E}$$

$$= \frac{5\text{V} - 0.7\text{V}}{2\text{ k}\Omega + 100 \times 1\text{k}\Omega} = \frac{4.3\text{V}}{102\text{ k}\Omega} = 0.042\text{mA}$$

∴ $$I_C = \beta I_B = 100 \times 0.042 = 4.2\text{ mA}$$

and $$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 15\text{V} - 4.2\text{mA}\,(470\Omega + 1\text{ k}\Omega) = 8.83\text{V}$$

∴ Operating point is **8.83V ; 4.2 mA.**

Now $$R_0 / R_E = 2\text{ k}\Omega / 1\text{ k}\Omega = 2$$

∴ Stability factor, $$S = (\beta + 1) \times \frac{1 + R_0/R_E}{\beta + 1 + R_0/R_E}$$

$$= (100 + 1) \times \frac{1 + 2}{100 + 1 + 2} = \mathbf{2.94}$$

9.14 Design of Transistor Biasing Circuits

(For low powered transistors)

In practice, the following steps are taken to design transistor biasing and stabilisation circuits :

Step 1. It is a common practice to take $R_E = 500 - 1000\Omega$. Greater the value of R_E, better is the stabilisation. However, if R_E is very large, higher voltage drop across it leaves reduced voltage drop across the collector load. Consequently, the output is decreased. Therefore, a compromise has to be made in the selection of the value of R_E.

Step 2. The zero signal current I_C is chosen according to the signal swing. However, in the initial stages of most transistor amplifiers, zero signal I_C = 1mA is sufficient. The major advantages of selecting this value are :

(*i*) The output impedance of a transistor is very high at 1mA. This increases the voltage gain.

(*ii*) There is little danger of overheating as 1mA is quite a small collector current.

It may be noted here that working the transistor below zero signal I_C = 1mA is not advisable because of strongly non-linear transistor characteristics.

Step 3. The values of resistances R_1 and R_2 are so selected that current I_1 flowing through R_1 and R_2 is atleast 10 times I_B *i.e.* $I_1 \geq 10\, I_B$. When this condition is satisfied, good stabilisation is achieved.

Step 4. The zero signal I_C should be a little more (say 20%) than the maximum collector current swing due to signal. For example, if collector current change is expected to be 3mA due to signal, then select zero signal $I_C \simeq 3.5$ mA. It is important to note this point. Selecting zero signal I_C below this value may cut off a part of negative half-cycle of a signal. On the other hand, selecting a value much above this value (say 15mA) may unnecessarily overheat the transistor, resulting in wastage of battery power. Moreover, a higher zero signal I_C will reduce the value of R_C (for same V_{CC}), resulting in reduced voltage gain.

Example 9.25. *In the circuit shown in Fig. 9.31, the operating point is chosen such that I_C = 2mA, V_{CE} = 3V. If R_C = 2.2 kΩ, V_{CC} = 9V and β = 50, determine the values of R_1, R_2 and R_E. Take V_{BE} = 0.3V and $I_1 = 10 I_B$.*

Solution. $$R_C = 2.2\text{ k}\Omega, \quad V_{CC} = 9\text{V}, \quad \beta = 50$$

$$V_{BE} = 0.3\text{ V}, \quad I_1 = 10\, I_B$$

As I_B is very small as compared to I_1, therefore, we can assume with reasonable accuracy that I_1 flowing through R_1 also flows through R_2.

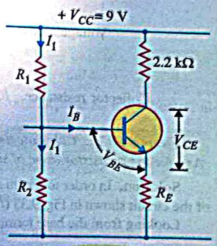


Fig. 9.31

Base current, $$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{50} = 0.04\text{ mA}$$

Current through R_1 & R_2 is

$$I_1 = 10\, I_B = 10 \times 0.04 = 0.4\text{ mA}$$

Now $$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

∴ $$R_1 + R_2 = \frac{V_{CC}}{I_1} = \frac{9\text{ V}}{0.4\text{ mA}} = 22.5\text{ k}\Omega$$

Applying Kirchhoff's voltage law to the collector side of the circuit, we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$